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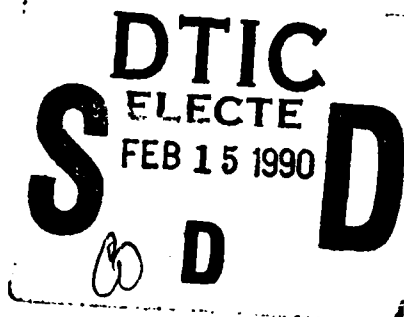
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Technical Document 1712
December 1989

Joint NOSC/NRL InP Microwave/Millimeter Wave Technology Workshop

Held at Naval Ocean Systems Center
San Diego, California 92152–5000 on
25–26 January 1989

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NAVAL OCEAN SYSTEMS CENTER
San Diego, California 92152–5000

J. D. FONTANA, CAPT, USN
Commander

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ADMINISTRATIVE INFORMATION

This document is a compilation of the papers delivered at the Joint NOSC/NRL InP Microwave/Millimeter Wave Technology Workshop. This workshop was held at the Naval Ocean Systems Center, San Diego, California, on 25 and 26 January 1989.

Released by
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Material and Device
Technology Branch

Under authority of
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Sciences Division

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CONTENTS

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AGENDA

InP MICROWAVE/MILLIMETER-WAVE TECHNOLOGY WORKSHOP

NOSC Meeting Coordinator	Hosts
Kitty Pitts Code 032	Louis Messick (Code 561) Naval Ocean Systems Center Ken Sleger (Code 6852) Naval Research Lab

Wednesday, 25 January

1300   Late Registration at the La Jolla Village Inn, Wind and Sea Rooms

Session I
Materials, Processing and Characterization
Chairman: M. Hollis, MIT Lincoln Laboratory

1330   Introductory Remarks - L. Messick, Naval Ocean Systems Center

1335   Recent Advances on the Growth of Bulk InP; G. Antypas, Crystacomm, Inc., Mountain View, CA.

1350   In-Chamber Characterization of Materials Properties During CVD Processing of III-V Compound and Alloy Semiconductors; D. L. Lile, R. Iyer, R. R. Chang and B. Bollig, Colorado State University, Ft. Collins, CO.

1405   In-Situ Rapid Isothermal Processing of II-A Fluorides for InP Based Devices; R. Singh, University of Oklahoma, Norman, OK.

1420   Encapsulated Rapid Thermal Annealing and Thin Gate Dielectrics for InP MISFETs; V. J. Kapoor, M. D. Biedenbender and G. J. Johnson, University of Cincinnati, Cincinatti, OH.

1435   Photoluminescence as a Technique for Assessing Thermal Damage and Implant Activation During Post-Implant Anneal of S1-Implanted InP; R. R. Chang and D. L. Lile, Colorado State University, Ft. Collins, CO.

1450   P/N Junction Vapor Phase Epitaxial Growth in InP and JFET Results with all Epitaxial Layer Growth; J. Crowley, Varian Associates, Santa Clara, CA.

1505   P-Doping with Maganese in MOVPE-GROWN InP and InGaAs; A. R. Clawson and T. T. Vu, Naval Ocean Systems Center, San Diego, CA.

1520   InP on GaAs/Si Substrates for Monolithic Integration of Advanced High-Speed Optoelectronics; S. M. Vernon, Spire Corporation, Bedford, MA.

1535   Downstream Plasma Activated Etching of III-V Compound Semiconductors; R. Iyer and D. L. Lile, Colorado State University, Ft. Collins, CO.

1550	Break
1620	Panel Discussion: Materials, Processing and Characterization Moderator: D. L. Lile, Colorado State University

Session II
Devices
Chairman: R. Singh, University of Oklahoma

1710	The Case for InP, In_xGa_xAs and In_yAs Heterojunction-Based MISFETs, SISFETs and MODFETs; H. H. Wieder, University of California, San Diego, CA.
1725	InAlAs/InGaAs Heterojunction Bipolar Transistors; U. Mishra*, A. S. Brown** and J. F. Jensen, Hughes Research Laboratory, Malibu, CA. *Now at North Carolina State University, Raleigh, NC. **Now at Army Research Office, Durham, NC.
1740	High Performance In,GaAs MODFETs on InP and GaAs; L. F. Eastman, Cornell University, Ithaca, NY.
1755	Gain and Noise Characteristics of InAlAs/InGaAs Strained HEMT's; D. Pavlidis, G. I. Ng and M. Weiss, University of Michigan, Ann Arbor, MI.
1810	End of Session
1900	Dinner

Thursday, 26 January

Session III

Devices
Chairman: J. Berenz, TRW

0830	Non-Stationary Transport Phenomena in Indium-Phosphide-Based Heterojunction Bipolar Transistors; J. Lucpelouard and M. A. Littlejohn, North Carolina State University, Raleigh, NC.
0845	Analytical and Computer-Aided Models of InP-Based MISFETs and Heterojunction Devices; A. J. Shey and W. H. Ku, University of California, San Diego, CA and L. Messick, Naval Ocean Systems Center, San Diego, CA
0900	A Study of Enhanced Barrier Schottky Gates for N-InP MESFETs; A. A. Iliadis and W. Lee, University of Maryland, College Park, MD and O. A. Aina, Allied-Signal Aerospace Company, Columbia, MD.
0915	Research on InP Devices at Lincoln Laboratory; A. R. Calawa, C. L. Chen, J. D. Woodhouse, S. C. Palmateer, S. H. Groves, G. W. Iseler, W. E. Courtney, and J. P. Donnelly, MIT Lincoln Laboratory, Lexington, MA.

0930   Highly Stable Microwave Performance of InP/InGaAs HIGFETs; E. A. Martin♦, O. A. Aina, A. A. Iliadis*, M. R. Mattingly, and E. Hemphling, Allied-Signal Aerospace Company, Columbia, MD. * University of Maryland, College Park, MD. ♦Also with the University of Maryland.

0945   Interface Processing for High Performance Insulated Gate Devices on InP; R. Chang, Z. Zou, K. Han, R. Iyer, and D. L. Lile, Colorado State University, Ft. Collins, CO.

1000   Break

1030   Multi-Channel InGaAs MESFETs Having Uniform DC and Microwave Gains; A. Fathimulla, H. Hier and J. Abrahams, Allied-Signal Aerospace Company, Columbia, MD.

1045   InP Junction FETs with a Nitride-Registered Gate Metallization; J. B. Boos, W. Kruppa* and B. Molnar, Naval Research Laboratory, Washington, DC. * George Mason University, Fairfax, VA and Sachs/Freeman Associates, Landover, MD.

1100   InP-Based Pseudomorphic High-Speed Devices Realized by Molecular Beam Epitaxy, P. Bhattacharya, University of Michigan, Ann Arbor, MI.

1115   A Diffused Junction InP JFET for High Speed Integrated Circuit and Power Applications; C. R. Zeisse, R. Nguyen, T. T. Vu, L. Messick, Naval Ocean Systems Center, San Diego, CA and K. L. Moazed, North Carolina State University, Raleigh, NC.

1130   Radiation Effects on InP-Based Electrical and Optical Devices; K. N. Vu, J. Y. Yaung, R. E. Helander, and G. B. Newstrom, TRW, Carson, CA.

Session IV

Applications and Devices
Chairman: B. Fank, Varian

1145   2-40 GHz InGaAs HEMT Monolithic Distributed Amplifier; J. Berenz, J. Yonaki, K. Nakano, M. LaCon and K. Stolt, TRW, Redondo Beach, CA and H. Wieder and P. Chu, University of California, San Diego, CA.

1200   GaInAs MISFET Wideband Microwave Power Amplifiers; D. Bechtle, L. C. Upadhyayula, P. D. Gardner and S. Y. Narayan, David Sarnoff Research Center, Princeton, NJ.

1215   Novel Applications of InP Based Technology: Neurocomputing; R. Singh, University of Oklahoma, Norman, OK.

1230   Lunch

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WORKSHOP SUMMARY

K. J. Sleger

Naval Research Laboratory
Washington, DC

InP MICROWAVE/MM-WAVE TECHNOLOGY WORKSHOP

25-26 January 1989 , NOSC

SESSION I

Materials, Processing

9 papers

1 panel session

SESSIONS II, III

Devices

15 papers

SESSIONS IV

Appliations and Devices

7 papers

1 panel session

Whither InP?

InP Workshop Participant Questions

1. Please state your interest in InP and derivative technolo-
gies? What is your business orientation (R/D, components, foun-
dry service, etc.)?

2. What, in your opinion, are the benefits and/or value added
features of InP and derivative technologies? What connections to
other technologies can you identify?

3. Is there a role for InP and derivative technologies in con-
necting diverse systems? Does the use of InP suggest new system
architectures and new circuits concepts which could change the
basis for competition?

4. What competitive products do you see emerging from the InP
and related technology effort currently underway at you organi-
zation? What InP and related technology R&D efforts do you plan
to pursue in the future? Do you see opportunities for InP to
change competitive balance with, say, GaAs?

5. What is the role of InP and related technologies in the solid
state RF/MW/MMW device/IC/module market place? Please include
responses to question 1-4 that apply to RF/MW/MMW solid state
devices/ICs.

6. What, in your opinion, represents the resource limits and
marketing barriers currently inhibiting the development of InP?

7. Have you identified users seeking the benefits of InP and
derivative technologies? In not, wry not? If so, which ones and
what are their needs?

→ TECHNICAL HIGHLIGHTS:

+ Drift problem with MIS devices under attack with epitaxial dielectrics, heat pulse processing, silicon substrates, silicon wedge dielectrics, gentle plasma etching, sulfidation (5% drift over 10⁵ sec, 4V drain, 4V gate), hydrogenation (2% drift)

+ Ion implantation damages to 3 microns or more even for the shortest anneal cycle

+ Limits to HJ device peformance related to epitaxial layer design (at present HBT working at 30% beta max)

+ Atomic planar doping in use for MODFET on InP with matching - V_{sat} about 1.6 - 1.8 x 10⁷ cm/sec

+ Small drain current drift observed in SiO2 based HIGFET-drift less than 4% over 15 hours

+ InAlAs-InGaAs planar-doped HEMTs latice matched to InP, 0-.25 micron T-gate, 900 mS/mm, 0.5 dB NF at 18 GHz

+ Hot Electron InP/InGaAs HBT f_t = 140 GHz, f_{max} = 70 GHz.

MATERIAL PANEL

+ Substrate perspective-niche technology/market with spawning potential

+ Defect-free material coming but market driven

+ The preferred choice for electro-optics

+ A good future for epitaxial HJ devices

+ Government has a lack of global planning

+ Do not wait or depend on government for success

14

DEVICE/APPLICATIONS PANEL

+ Substrate is not the problem

+ Results at 1988 IEDM demonstrated the winning properties of InP-its up to us to carry the ball

+ Understanding **NOW** is the key to success

+ CAD above 40 GHz may be a stumbling block

+ We have InP *art* not technology

+ Optics is the market driver

+ ICs can trample material efforts

+ Cost/penalty function could be a problem

+ Basic science needs strengthening, especially in reliability and reproducibility

+ Need to establish a material team to contain the cost of InP substrate

+ Remember the moving FERMI level in silicon and how it was "fixed"

15

WHITHER INP?

IDENTIFIED APPLICATIONS

Terminal guidance

Weather satellite radiometer

Interface to HDTV

LNS-high bandwidth interconnect

Optically controlled phased array steering

Radiation hard electronics

Combining diverse functions

RECOMMENDATIONS

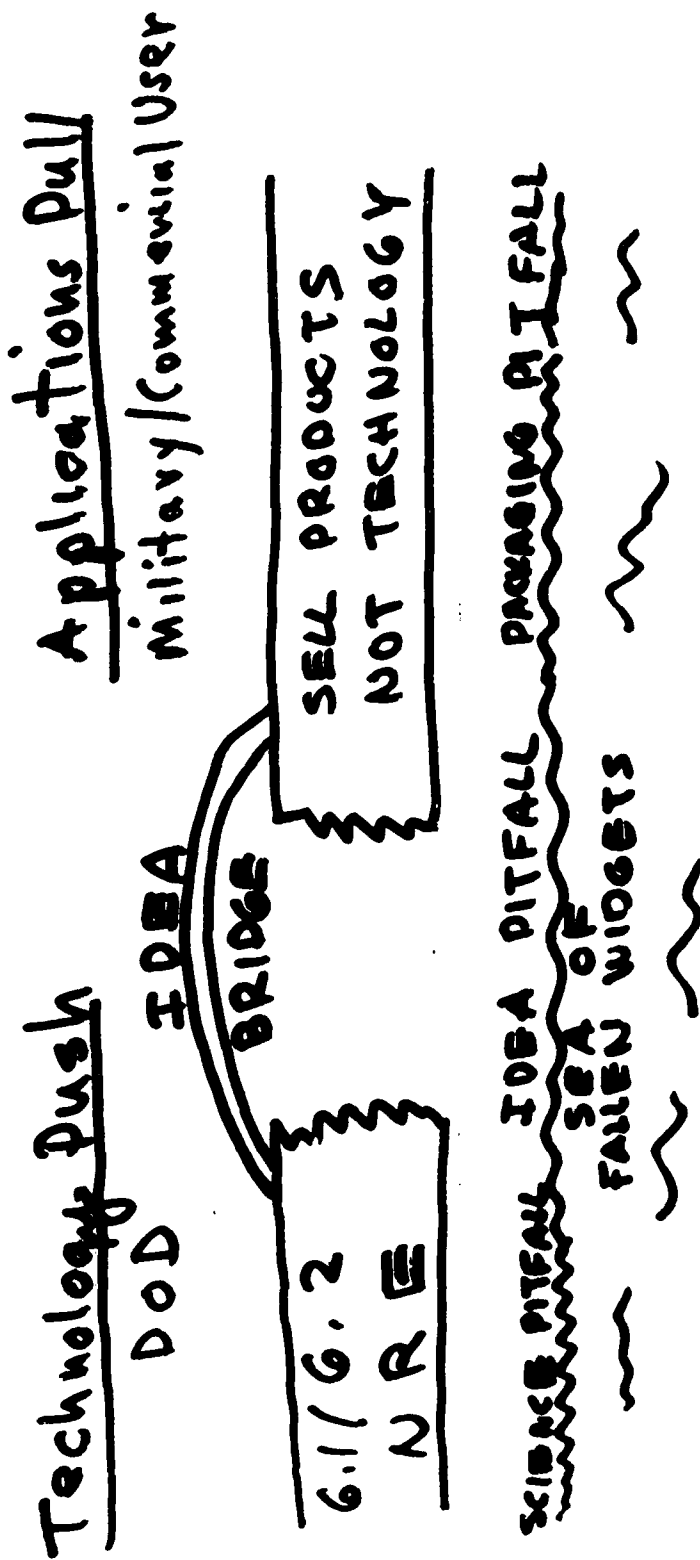Concentration on surface passivation and gate insulator

Package for success!

TODAY'S PRODUCTS

MMWave tranceiver

CMOS equivalent InGaAs

ACTION

Schedule a brainstorming session

Establish MISFET committee

16

Whither InP?

Technology Push
DoD

Applications Pull
Military/Commercial User

IDEA

BRIDGE

6.1/6.2 NRE

SELL PRODUCTS NOT TECHNOLOGY

SCIENCE PITFALL   IDEA PITFALL   PRODUCT PITFALL

SEA OF FALLEN WIDGETS

Typical Benefits:

Military
Cost, Survivability, reliability, Maintainability, Performance, size, weight (efficiency), wide dynamic range, high temperature operation

Commercial
Affordability, consumable fun, pleasure, hope, save time, sure energy, transportation, storage, mobility, autonomy

IN CHAMBER CHARACTERIZATION OF MATERIALS PROPERTIES DURING CVD PROCESSING OF III-V COMPOUND AND ALLOY SEMICONDUCTORS

D. L. Lile, R. Iyer, R. R. Chang and B. Bollig

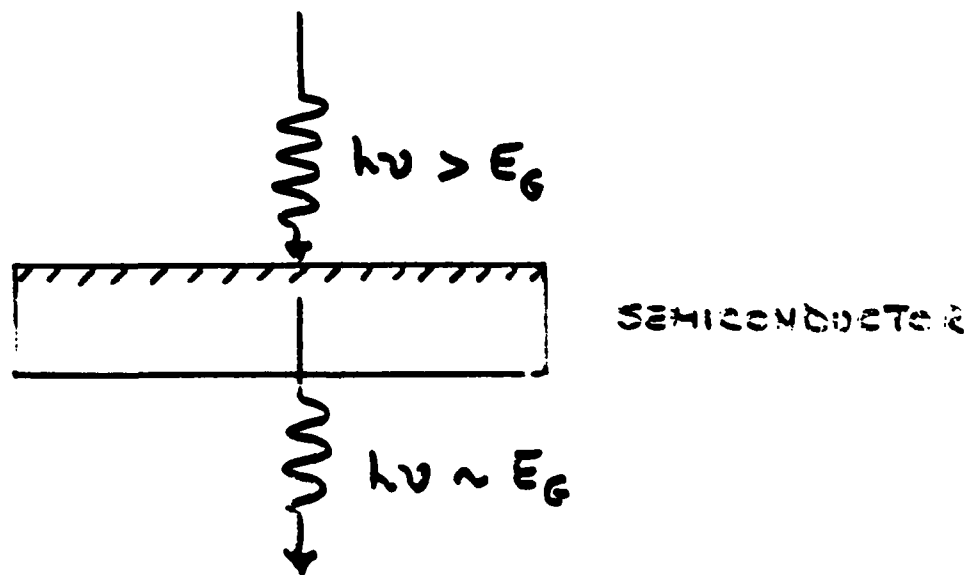Colorado State University
Fort Collins, CO

PRESENT APPROACH

```
┌─────────────────────┐      ┌─────────────────┐      ┌──────────────────────┐
│  STARTING WAFER     │──────│  PROCESS -      │──────│  FINISHED DEVICE     │
│                     │      │  CVD,MBE etc.   │      │                      │
└─────────────────────┘      └─────────────────┘      └──────────────────────┘
          ▲                                                       ▲
          │                                                       │
   CHARACTERIZATION                                        CHARACTERIZATION
```

PROPOSED APPROACH

```
                            ┌──────────────────┐
                            │  RAMAN           │
                            │  SPECTROSCOPY    │
                            └──────────────────┘
                                                    ┌────────────────────┐
                                                    │ PHOTOLUMINESCENCE  │
                                                    └────────────────────┘

                            ┌──────────────────┐
  ┌─────────────────────┐   │  PROCESS-        │   ┌────────────────────┐
  │  STARTING WAFER     │───│  CVD,MBE etc.    │───│  ELLIPSOMETRY      │
  └─────────────────────┘   └──────────────────┘   └────────────────────┘
          ▲
          │
   CHARACTERIZATION
                            ┌──────────────────┐
                            │  MASS            │
                            │  SPECTROSCOPY    │
                            └──────────────────┘

                                        ┌────────────────────┐
                                        │  FINISHED DEVICE   │
                                        └────────────────────┘
                                                 ▲
                                                 │
                                          CHARACTERIZATION
```

21

RAMAN
SPECTRUM

PHOTOLUMINESCENCE
SPECTRUM

ELLIPSOMETRIC
DATA

RUDOLPH AUTOMATIC
ROTATING ANALYZER

GAS SUPPLY

SPEX
TRIPLEMATE
SPECTROGRAPH

He-Ne
LASER

CVD CHAMBER

RHEED

BALTZERS
RGA

ARGON ION LASER

TUNGSTEN IODINE
SOURCE

ISOLATION MOUNTED
OPTICAL TABLE

BALTZERS HIGH PRESSURE
TURBOMOLECULAR PUMP

22

PHOTOLUMINESCENCE

$h\nu > E_G$

SEMICONDUCTOR

$h\nu \sim E_G$

SPACE CHARGE
WIDTH

$$I = I_0(s) \, EXP\left[-W/d\right]$$

ABSORPTION
LENGTH

hv>Eg

CONDUCTION BAND EDGE

PL, $hv'=Eg$

VALENCE BAND EDGE

SPACE CHARGE
DEPLETION WIDTH, W
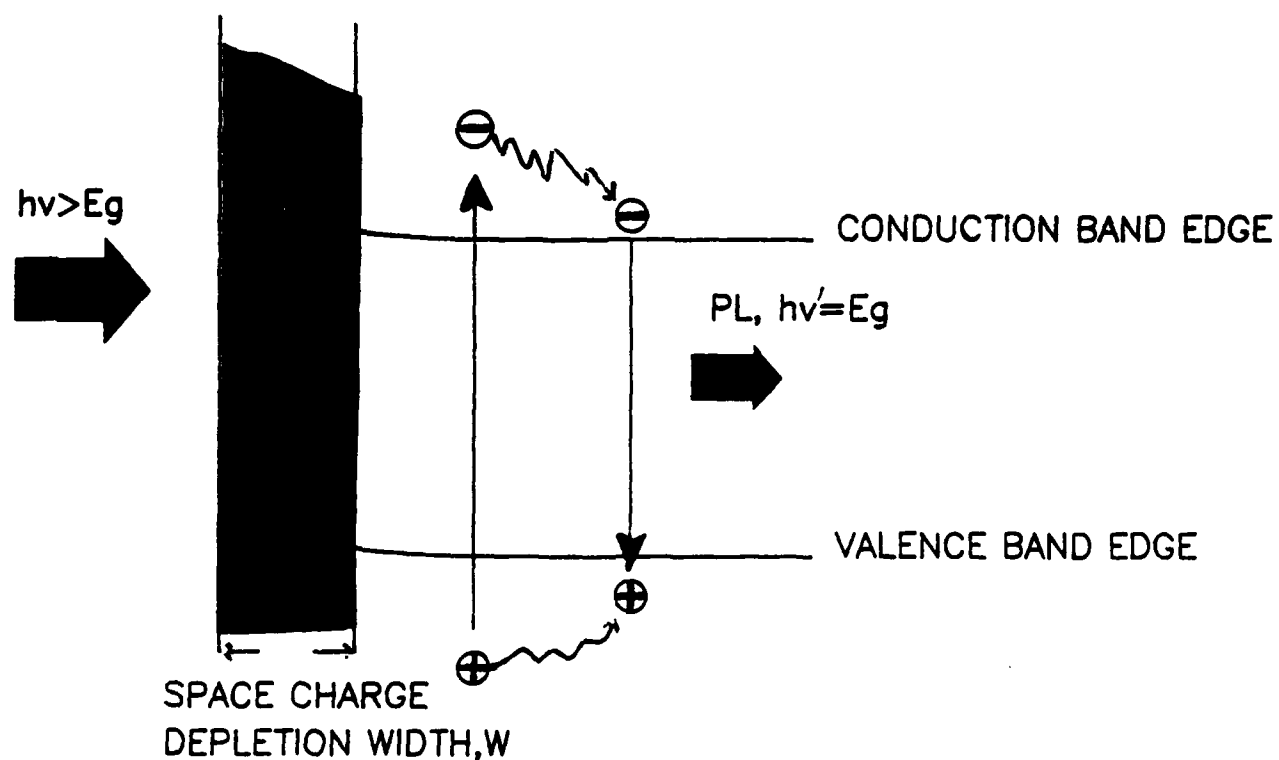
PHOTOLUMINESCENCE INTENSITY AFFECTED BY:

1. SURFACE RECOMBINATION, S
2. SPACE CHARGE LAYER, W

$$I = I_e(S, V_s) * EXP(-W \cdot \alpha)$$

5 mW He–Ne Laser

Anode

LS–700 Filter

Pt Cathode

InP Sample

PVC

Teflon Seal

O–Ring

Silicon p–i–n

Electrolyte or Etching Solution

Transimpedance Amplifier

Voltmeter

25
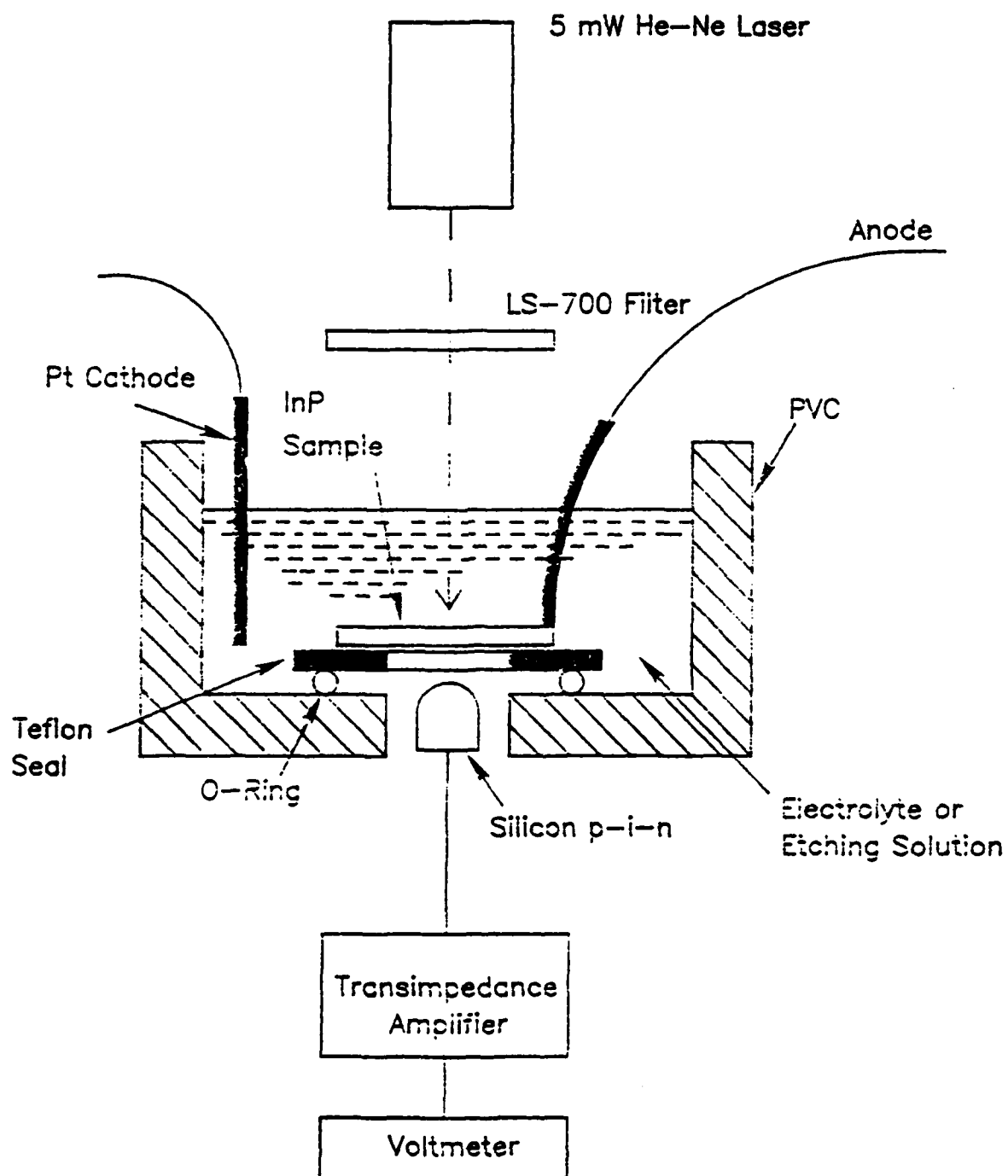
Chemical Treatment   In-Situ Photoluminescence

(Relative intensity normalized to NRL surface)

As polished (Br MeOH)——————————————— 0.4

NRL———————————————————————— 1.0

HNO3————————————————————————— 0.9

HF——————————————————————————— .8

Iodic Acid—————————————————————— 0.32

KOH(in MeOH)———————————————————— 0.5~0.1 (unstable)

H2O2————————————————————————— 0.04

NH4OH————————————————————————— 0.3

300 C annealing———————————————————— 0.4

in Ar(30 min)

*Samples previously polished and etched in NRL solution.

Photoluminescence (arbitrary units)

1   .8   .6   .4   .2   0

(a)

(b)

(c)

Wavelength(nm)

300 400 500 600 700 800 900 1000 1100 1200

1   .8   .6   .4   .2   0

Responsivity (A/W)

TO PUMP

LASER

AMPLIFIER

PIN Si
DETECTOR

He-Ne LASER

SAMPLE

SHIELDED QUARTZ
LIGHT PIPE

STAINLESS STEEL
SUPPORT

FURNACE

GAS
INLET

28

Photoluminescence (arbitrary units) vs Time (SEC)

Photoluminescence vs Annealing Temperature(C)

(a) (b) (c) (d)

30
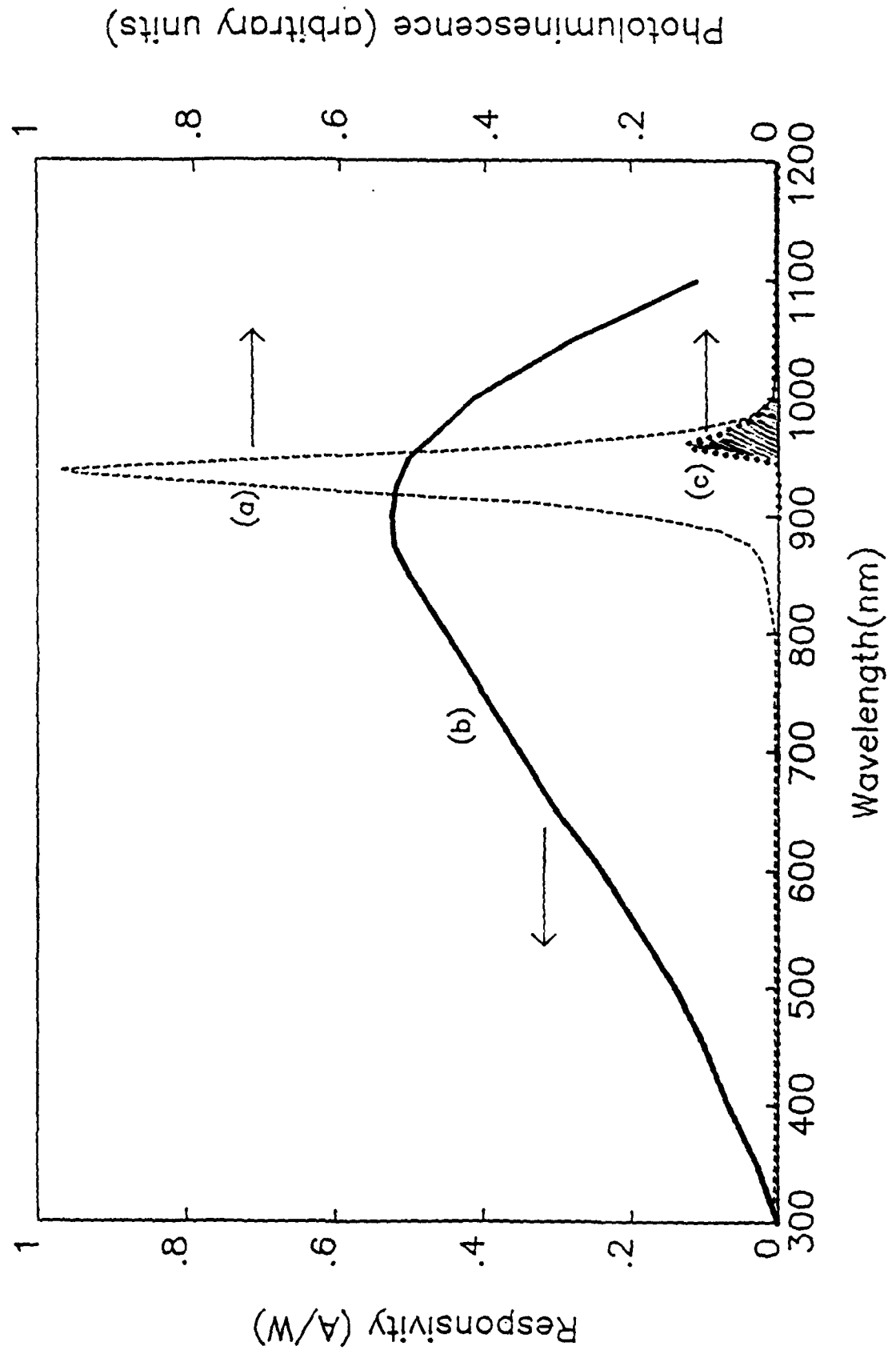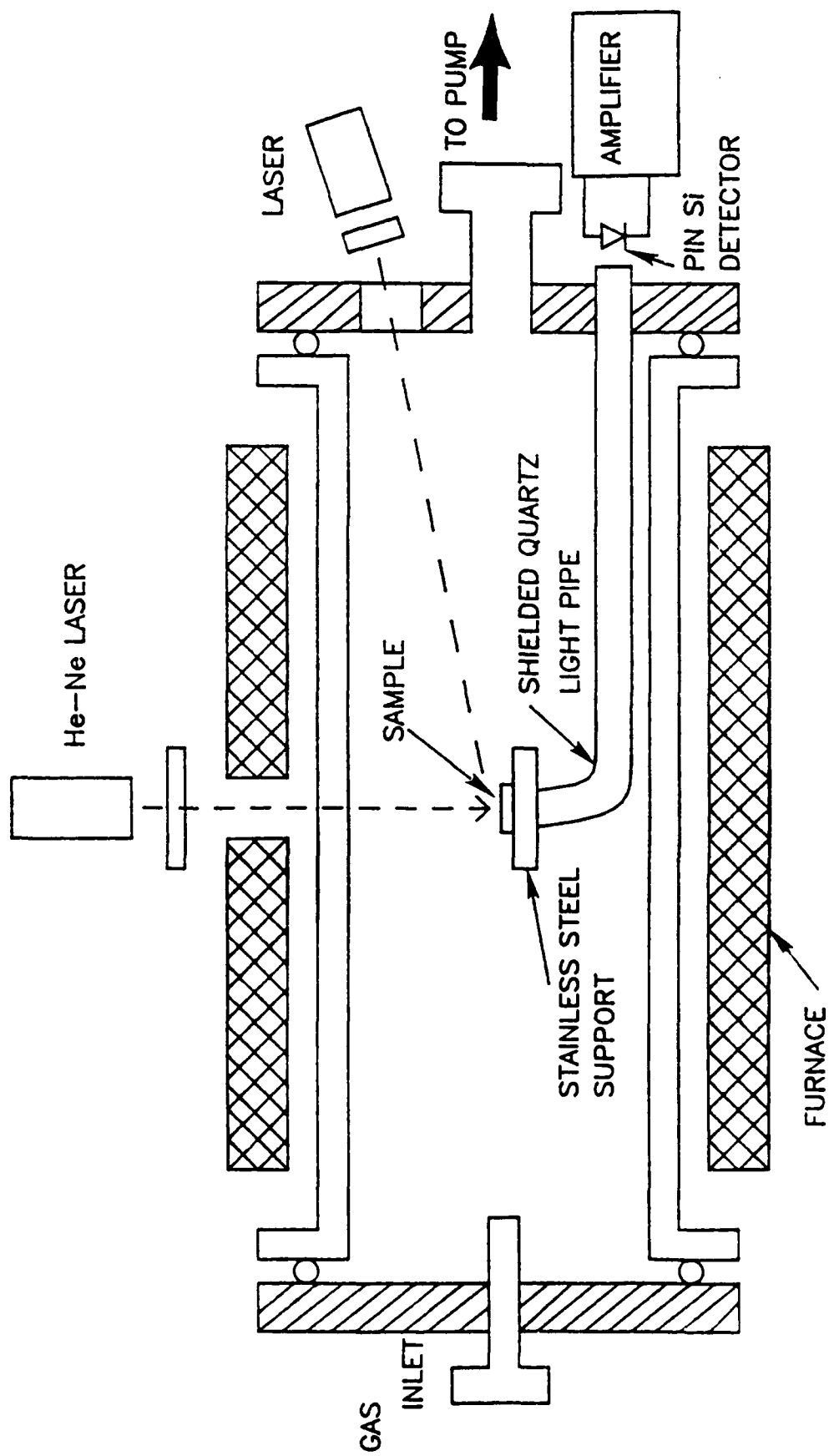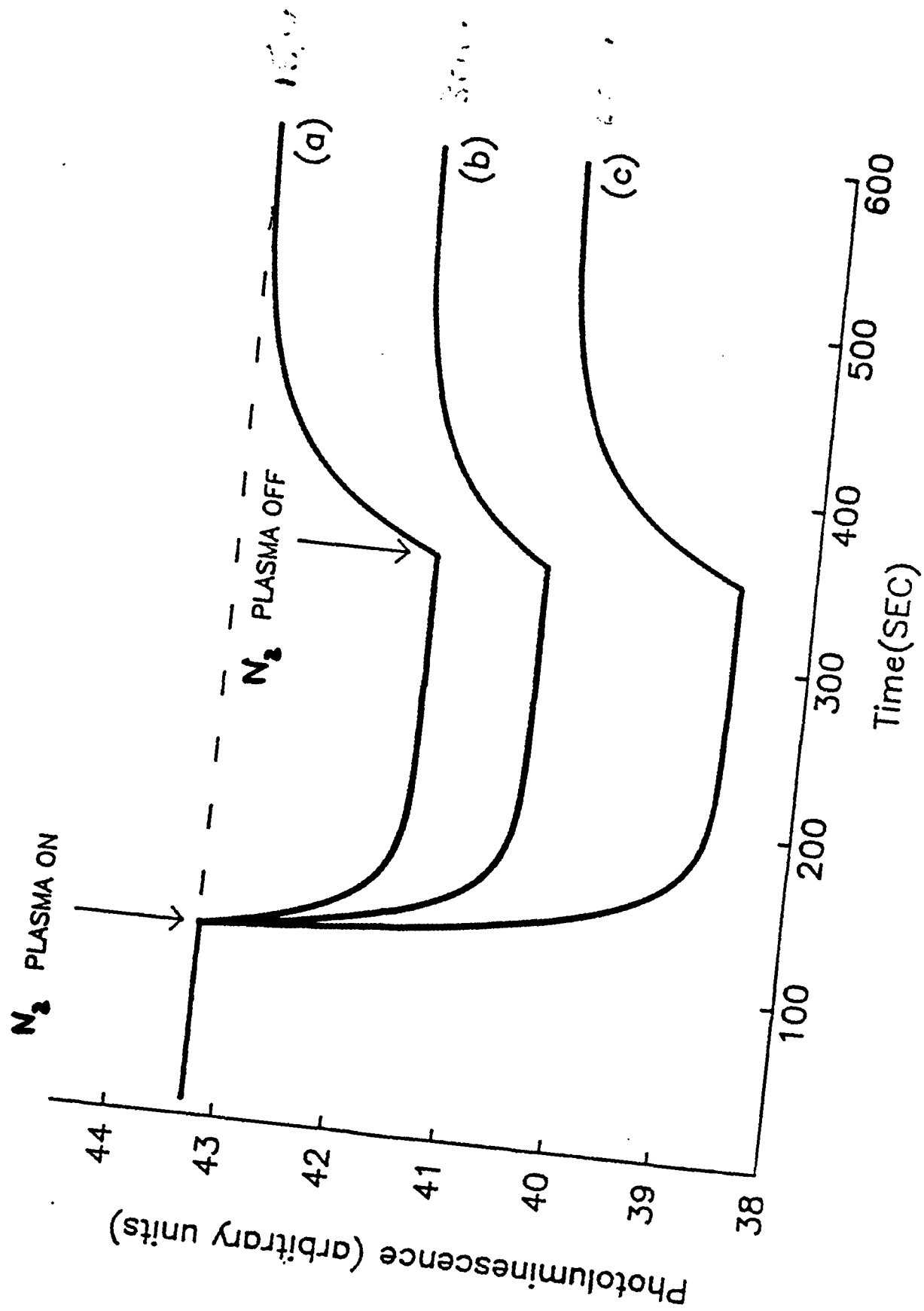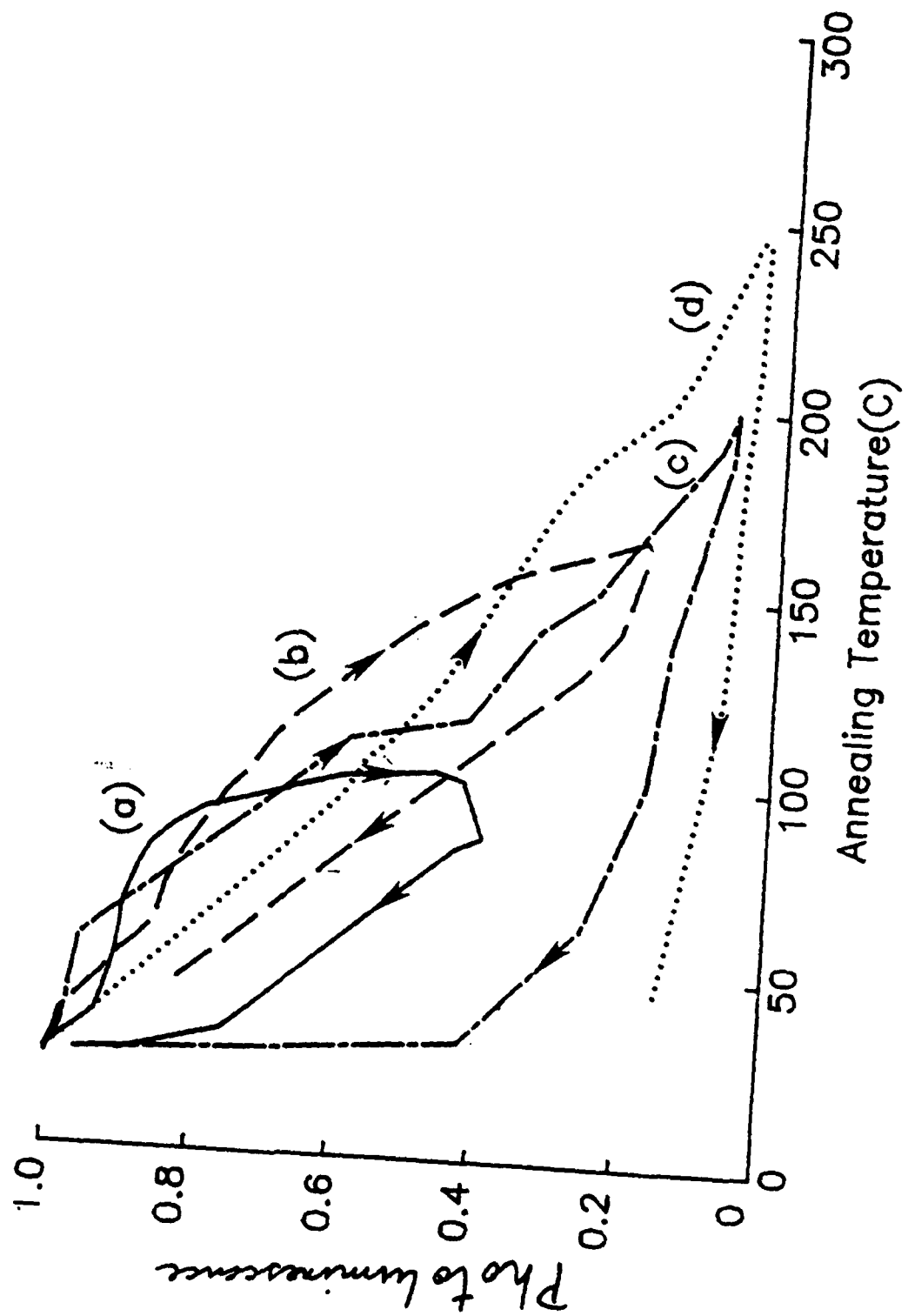
IN SITU PHOTOLUMINESCENCE RESPONSE DURING
TEMPERATURE CYCLING AT 400mTorr TO 250° C
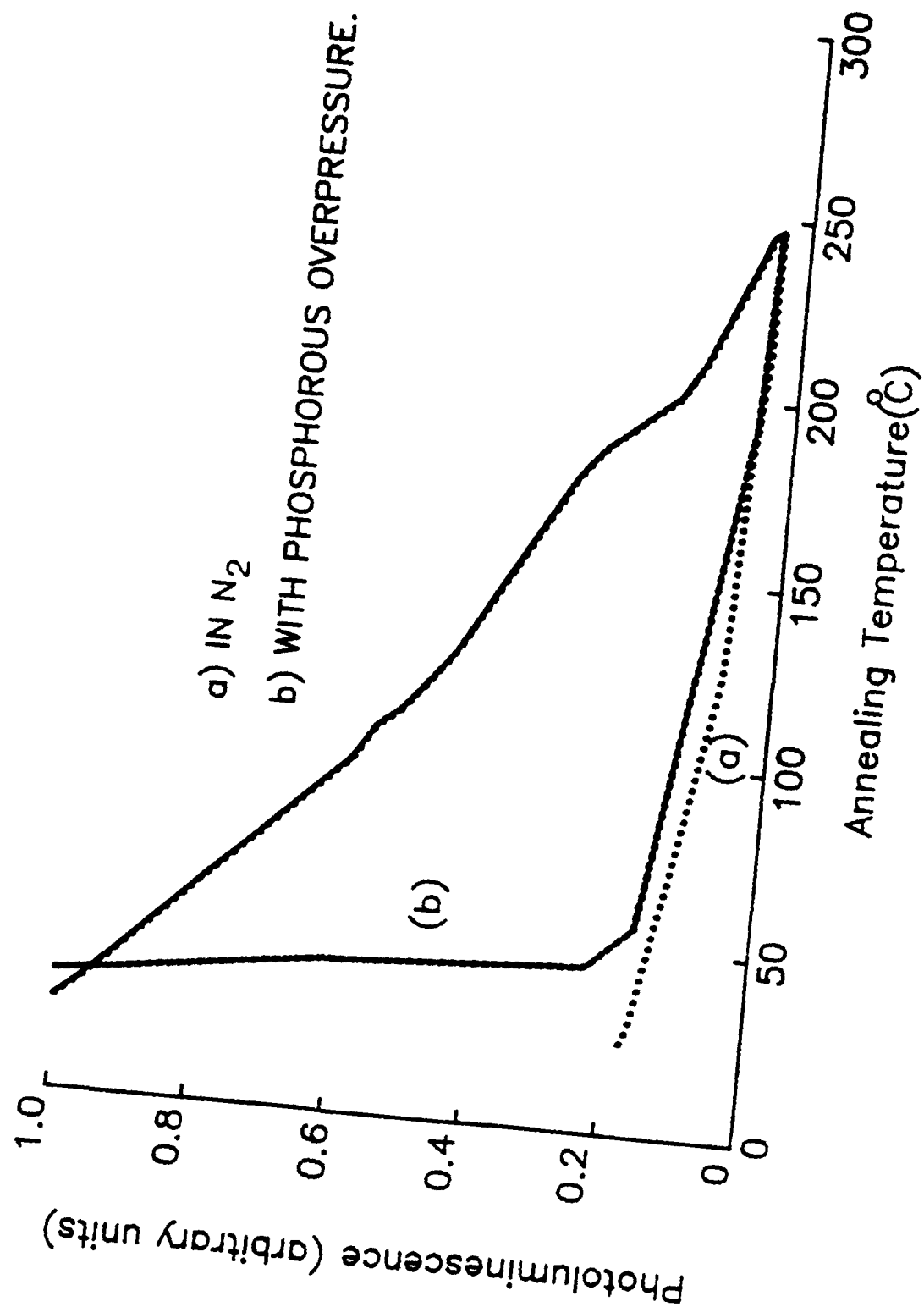
a) IN N$_2$
b) WITH PHOSPHOROUS OVERPRESSURE.

(b)

(a)

Annealing Temperature (°C)

Photoluminescence (arbitrary units)

1.0   0.8   0.6   0.4   0.2   0

50   100   150   200   250   300

IN-SITU RAPID ISOTHERMAL PROCESSING OF II-A FLUORIDES
FOR InP BASED DEVICES

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Computer Science
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IN-SITU RAPID ISOTHERMAL PROCESSING OF II-A FLUORIDES FOR InP BASED DEVICES

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EPITAXIAL DIELECTRICS
(A Relatively New Class of Dielectrics)

- II-A FLUORIDES (CaF_2, BaF_2, SrF_2 and their mixtures)

- LATTICE MATCH TO MOST IMPORTANT SEMICON-DUCTORS (Slight mismatch can be used for strained super lattice approach)

- COMPARED TO AMORPHOUS DIELECTRICS ORDERED SEMICONDUCTOR–DIELECTRIC INTERFACE
    - (1) Improved carrier transport (high mobility)
    - (2) Higher mobilities of electrons and holes in the dielectric is expected to provide improved hot carrier and rad. hardening feature

- SEMICONDUCTOR, DIELECTRIC, CONDUCTOR (SILICIDE e.g. $NiSi_2$) AND SUPERCONDUCTORS ALL POSSIBLY CAN BE GROWN IN ANY DESIRED SEQUENC

    - (1) True 3–D circuits with the capability of having interconnections both on top and bottom of the device
    - (2) Near femto second hybrid superconductor/semi-conductor switching transistors
    - (3) Integration of microelectronic, opto electronic and superconducting devices on one chip

- AS A GATE DIELECTRIC MATERIAL COMPARED TO SiO_2
    - (1) Large band gap ($\sim$ 12.0 eV)
    - (2) Ionic bond (stronger than covalent bond)
    - (3) Higher Dielectric Constant ($\sim$ 7.2)

Table: Epitaxial Alkaline Earth Flouride Semiconductor Systems

Fluoride	Semiconductor	Substrate Orientation	Lattice Mismatch(%)
CaF_2	Si	(100), (110), (111)	+0.61
SrF_2	InP	(100)	−1.2
$Ca_xSr_{1-x}F_2$	GaAs	(100), (110), (111)	0
$Ba_xSr_{1-x}F_2$	InP	(100)	0
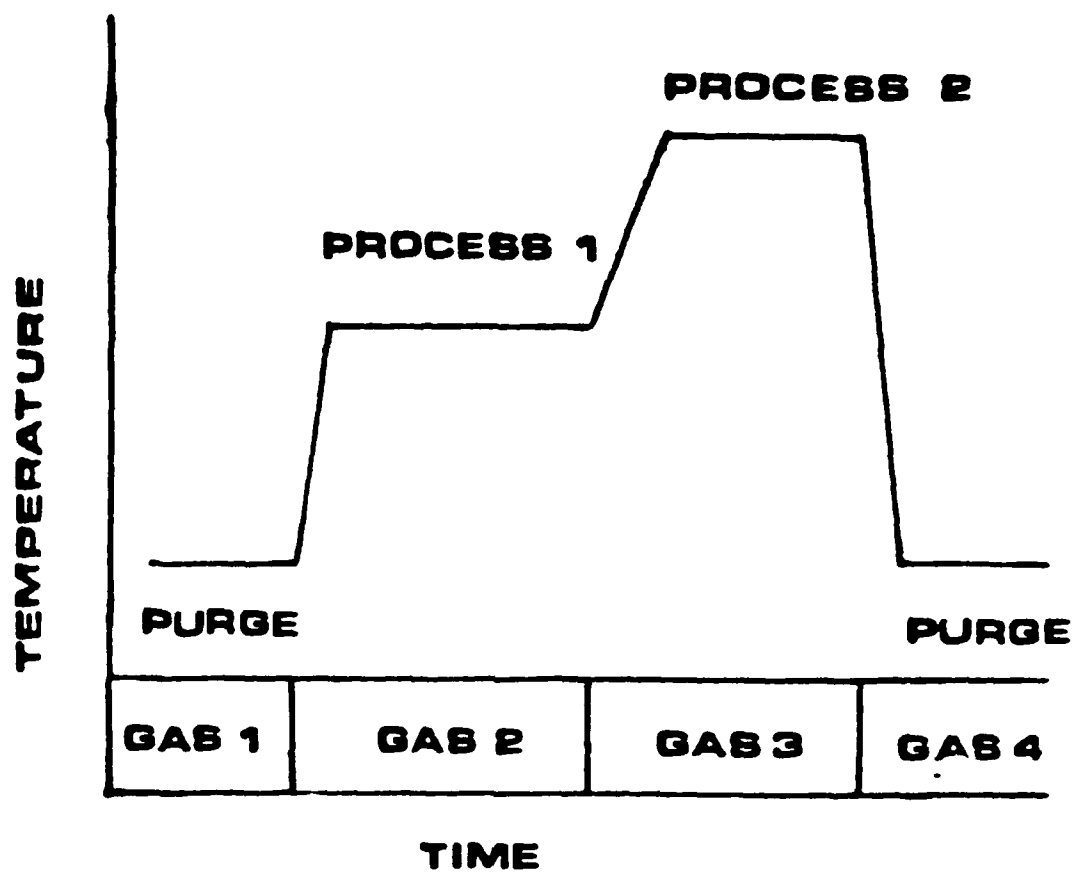
HETRO PRCESSING PROVIDES

PRECISE CONTROL : MATERIAL

                COMPOSITION

            : STRUCTURAL PROPERTIES

            : ELECTRICAL PROPERTIES

HEAT PULSE PARAMETER
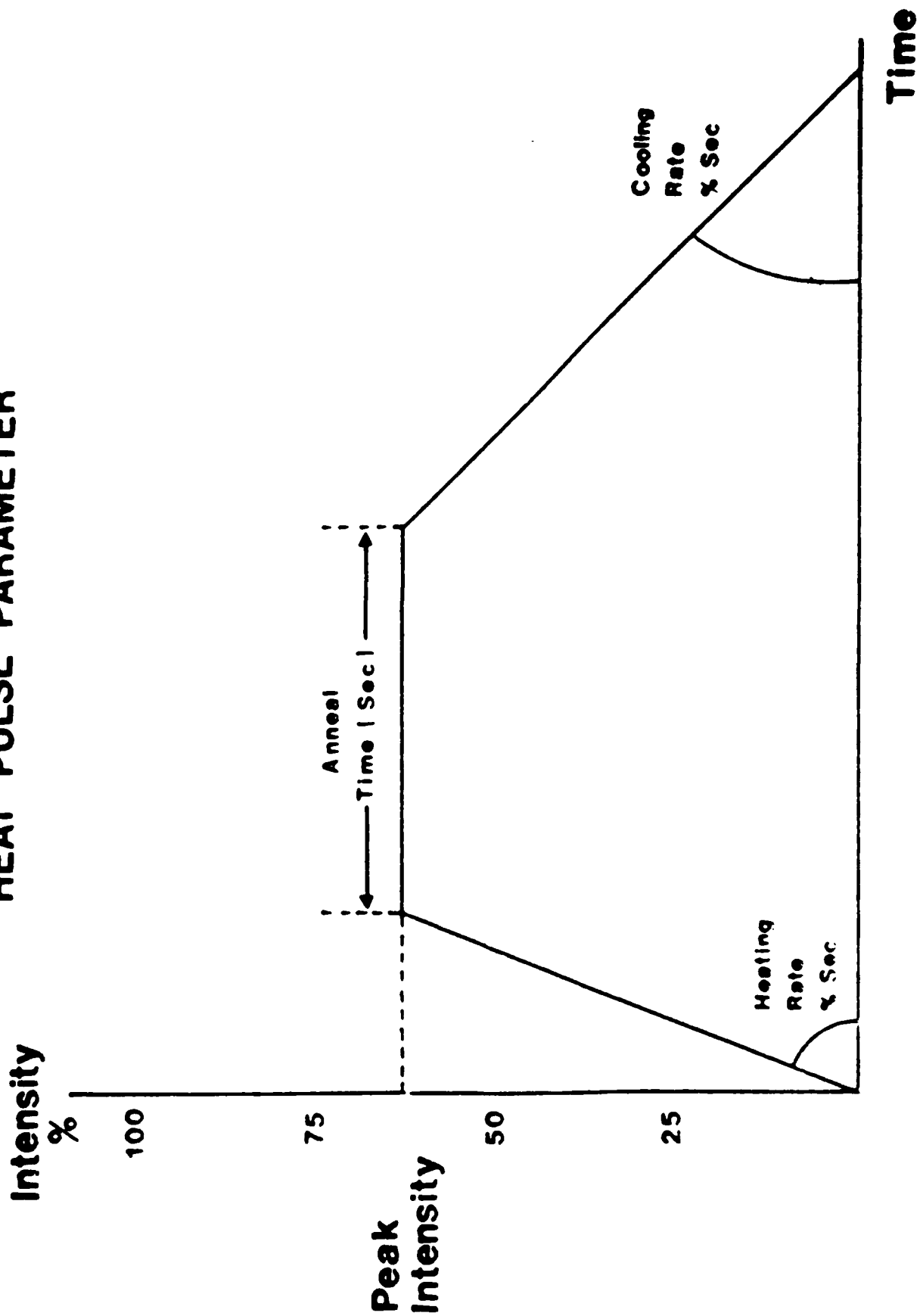
WATER COOLED LAMP REFLECTOR ASSEMBLY
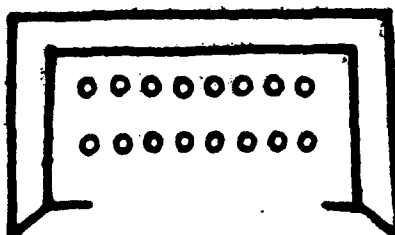
QUARTZ WINDOW

QUARTZ SAMPLE HOLDER

SAMPLE

CANTILEVER TC

EVAPORATION SOURCE

TURBOMOLECULAR PUMPING STATION
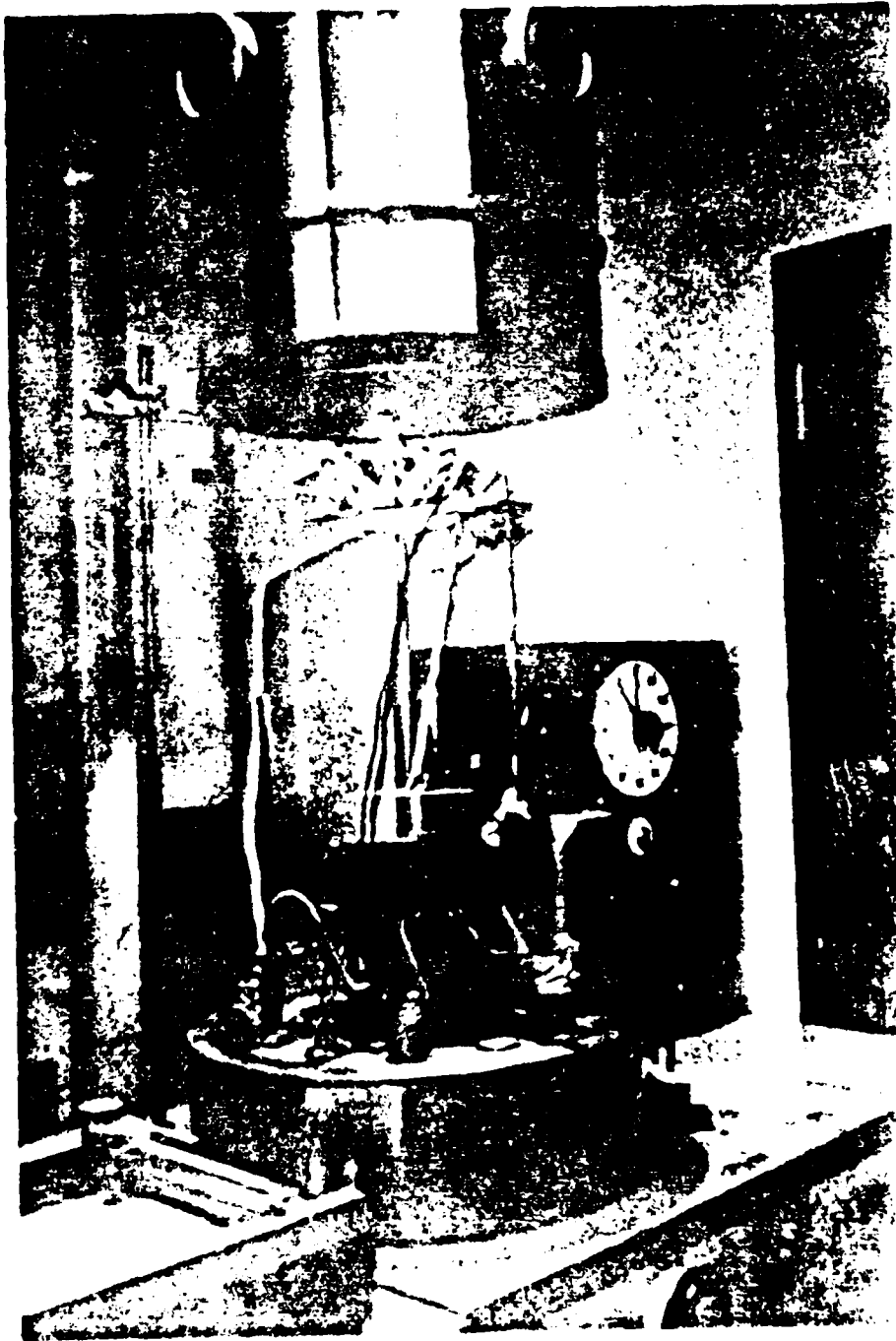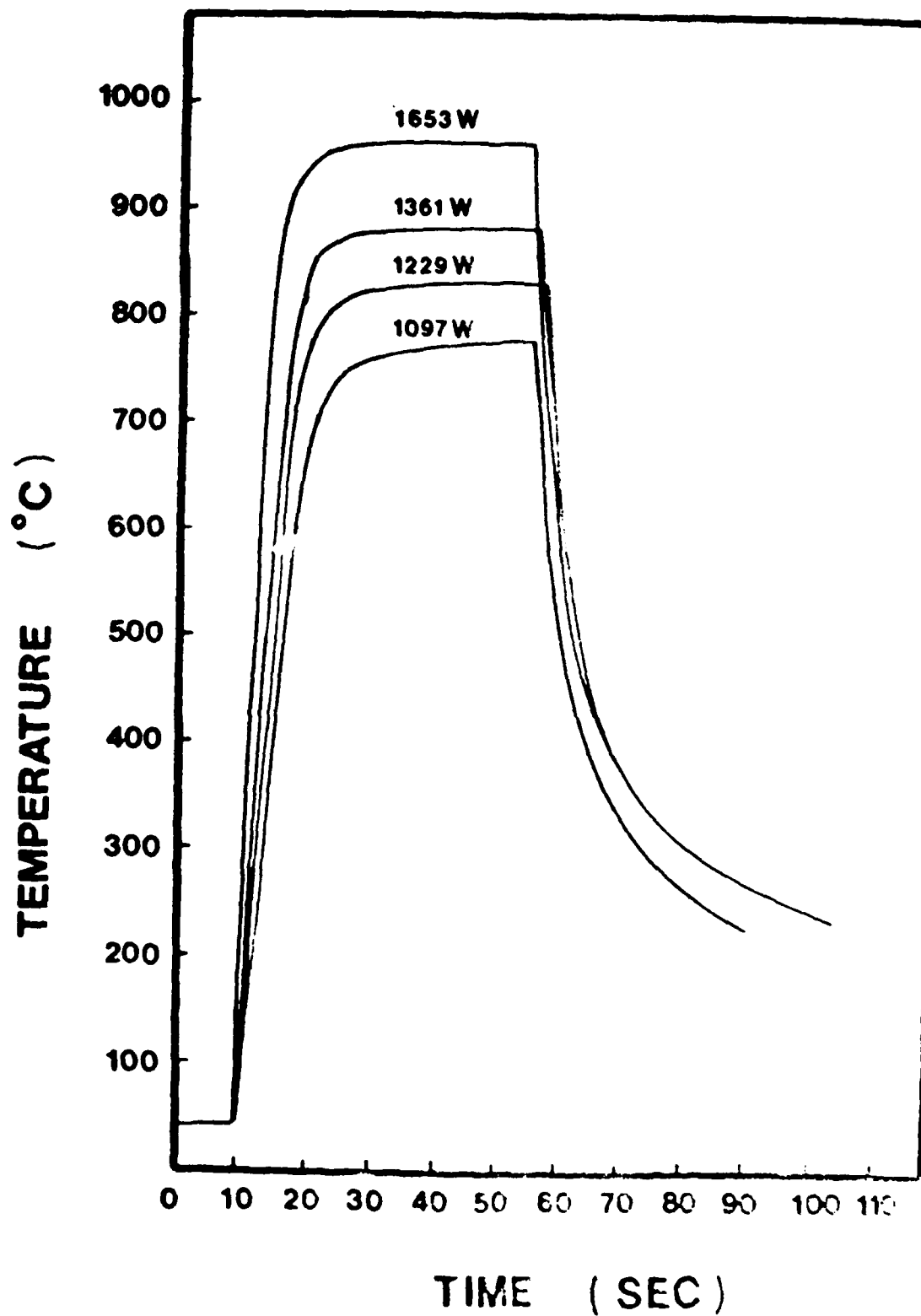
Fig. 1. Temperature - time cycles as a function of lamp power.

PROCESSING CONSIDERATIONS

(A) FURNACE PROCESSING (700–800°C HEATING FOR SEVERAL MINUTES)

- Diffusion Assisted Chemical Reactions Preferential Evaporation of Fluorine

```
                    ┌──────────────────────┐
                    │ Non-stoichiometric And│
                    │ Disordered Interface  │
                    └──────────────────────┘
                              │
        ┌─────────────────────────────────────────┐
        │ Electrically Active Defects Leads        │
        │ To Instability, Poor Carrier Transport   │
        │ And Limited Long Term Reliability        │
        └─────────────────────────────────────────┘
```

(B) IN-SITU RAPID ISOTHERMAL PROCESSING

```
┌──────────────┐
│ Load Wafer Into│
│ E-Beam System │
└──────────────┘
       │
┌─────────────────────────────────────┐
│ In-Situ Rapid Isothermal Cleaning   │
└─────────────────────────────────────┘
       │
┌──────────────────────────────────────────────┐
│ Deposition (~ 30–50 Å) Fluoride At Room Temp. │
└──────────────────────────────────────────────┘
       │
┌─────────────────────────────────────┐
│ In-Situ Rapid Isothermal Annealing  │
└─────────────────────────────────────┘
       │
┌──────────────────────────────────────────────┐
│ Deposit Desired Thickness of Fluoride at Room Temp. │
└──────────────────────────────────────────────┘
       │
┌────────────────┐        ┌──────────────────────────────┐
│ In-situ Annealing │ ──→  │ Measure Structural Properties │
└────────────────┘        └──────────────────────────────┘
       │
┌──────────┐
│ Metalize │
└──────────┘
       │
┌──────────────────────────────┐
│ Measure Electrical Properties │
└──────────────────────────────┘
```

eV

6.20 eV (2000Å) — — — → [~ **cutoff wavelength of tungsten-halogen lamp**]

6.0

$600\,/\,L$

Far
UV

Ground State   Ground State
Oxygen   Oxygen
Molecule   Atom
↓   ↓   ↓

5.115 eV (2424Å) → $\boxed{O_2(^3\Sigma_g^-) \longrightarrow O(^3P) + O(^3P)}$

5.0

4.25 eV (2920Å) → [Si V.B. → SiO_2 C.B. Transition]

4.14 eV (3000Å) — — — → $\boxed{O_2(^1\Delta_g) \to O(^3P) + O(^3P)}$

4.0

Near
UV

[SnO_2 Band Gap]
3.53 eV (3510Å)

3.49 eV (3550Å) → $\boxed{O_2(^1\Sigma_g^+) \to O(^3P) + O(^3P)}$

3.18 eV (3900Å)

3.0

3.15 eV (3940Å) → [Si C.B. → SiO_2 C.B. Transition]

Visible

2.0 1.964 eV (6300Å) ——— $\boxed{O(^3P) \to O(^1D)}$

1.628 eV (6719Å) → $\boxed{O_2(^3\Sigma_g^-) \longrightarrow O_2(^1\Sigma_g^+)}$

1.61 eV (7700Å)

Near
IR

[Si Band Gap]
1.12 eV (1.11μ)

1.0 0.977 eV (1.27μ) → $\boxed{O_2(^3\Sigma_g^-) \longrightarrow O_2(^1\Delta_g)}$

0.83 eV (1.5μ) — — —

Middle
IR

0.651 eV (1.90μ) → $\boxed{O_2(^1\Delta_g) \to O_2(^1\Sigma_g^+)}$

0.34 eV (3.6μ) → [I_{max} of 800°K black-body rad.]

0.21 eV (6.0μ) — — —

0   0.0576 eV $(21.5 \ldots$

CaF$_2$

Thickness = 100 Å

$N_{fb} = 1 \times 10^{10}$

VOLTAGE (V)

FIG: 1MHZ C-V CHARACTERISTICS OF 100Å CaF$_2$ ON SILICO

CaF$_2$ Thickness = 100 Å

% of samples

BREAK DOWN FIELD (MV/cm)

Figure 1

Figure 1 c)

● Si

x CaF$_2$ I

o CaF$_2$ II

b)

c)

a)
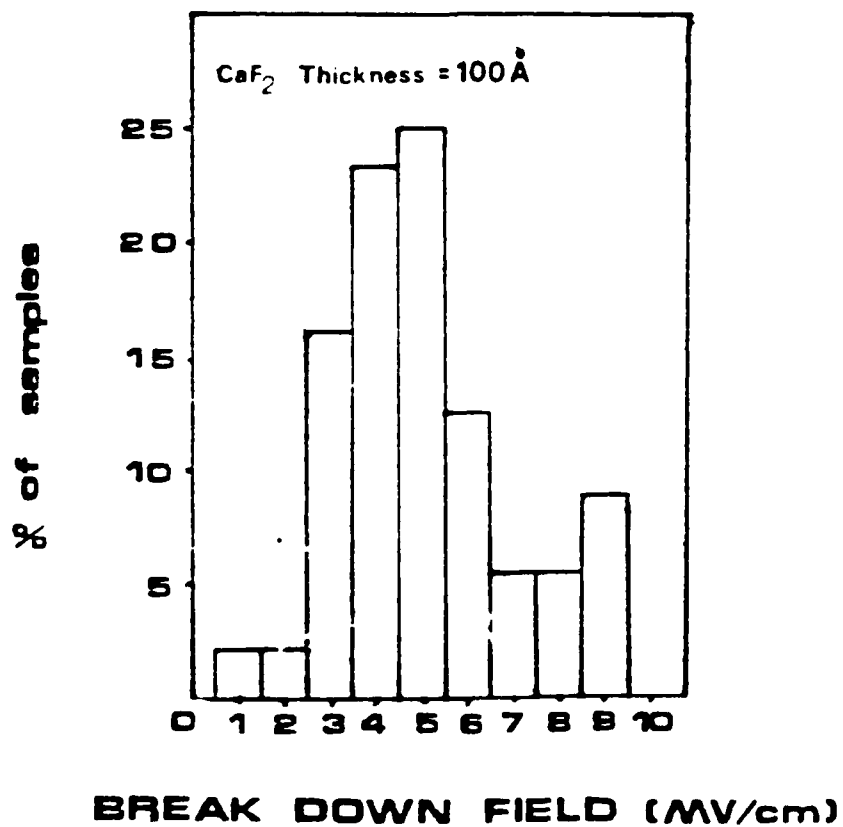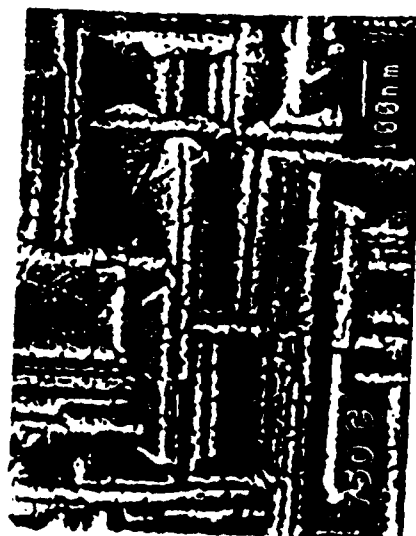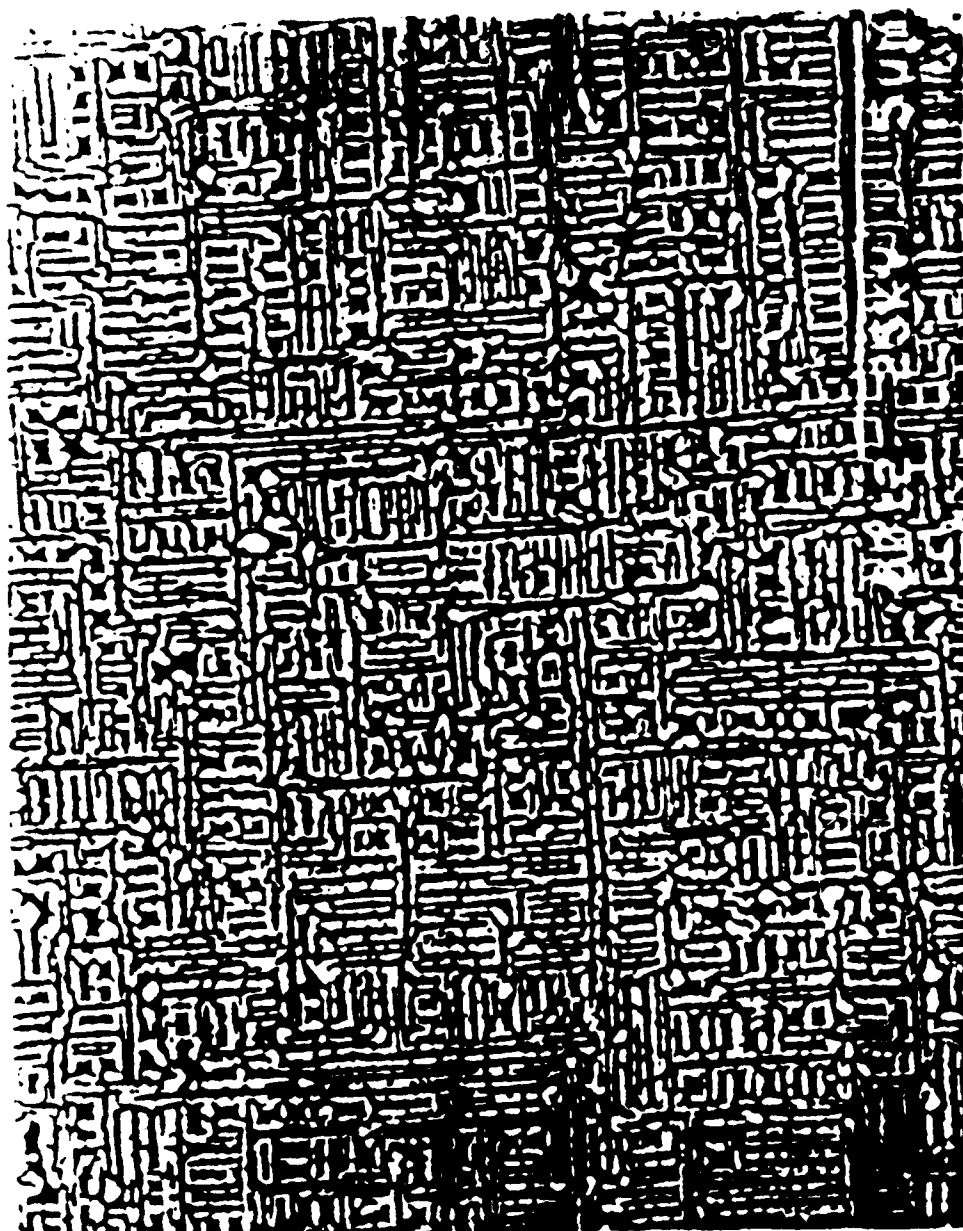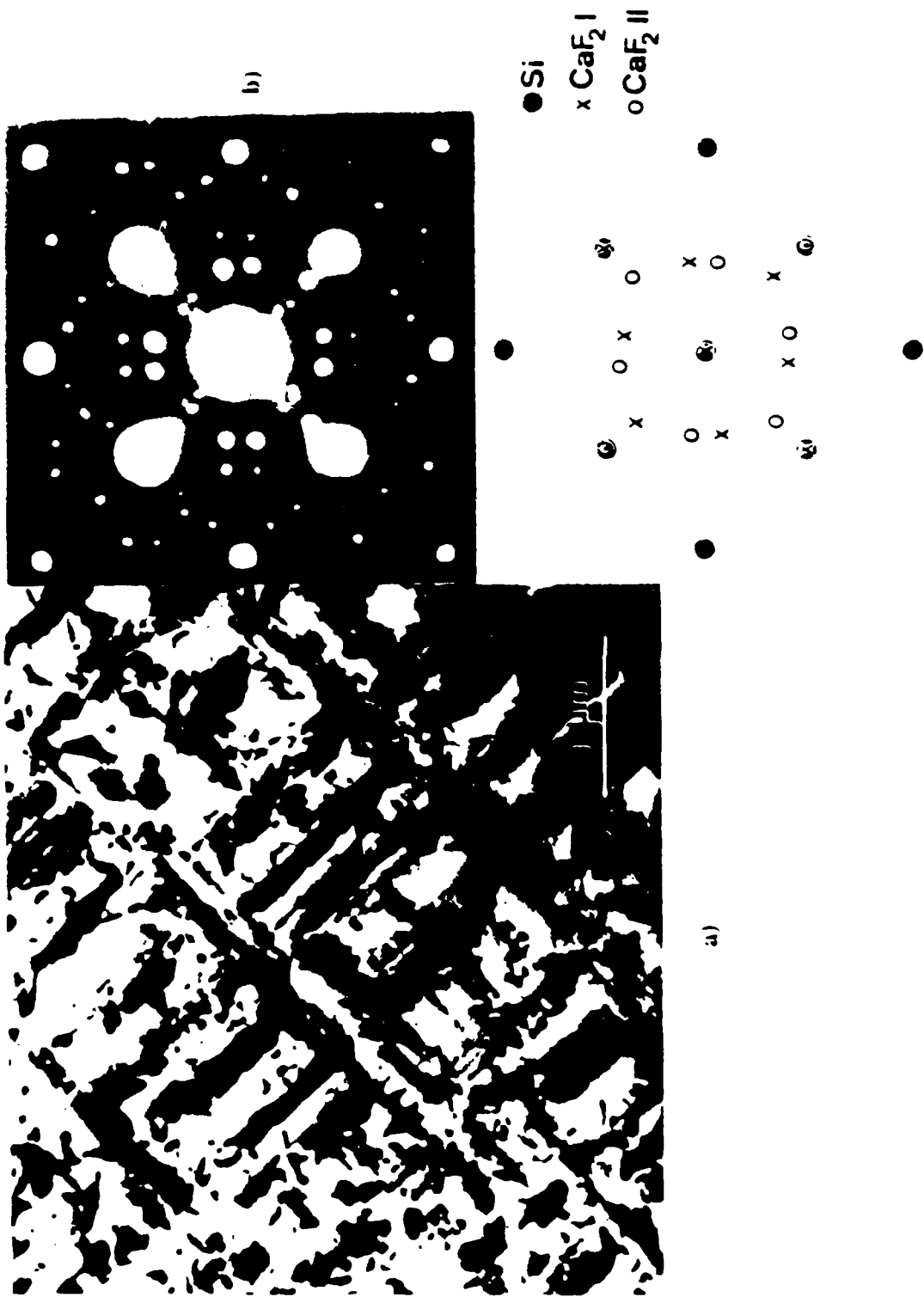
Figure 2

InP RESULTS

SAMPLE #	HISTORY OF SAMPLE	FRONT ψ	BACK ψ	FRONT Δ	BACK Δ	
Bare		11.23	11.23	140	140	
I_{31}	500λ 830°C, 30 sec 500λ 800°C, 15 sec	7.11	7.945	147.65	137.49	~ 1000λ
I_{32}	500λ 700°C, 10 sec 500λ 600°C, 15 sec	13.55	12.71	142.45	101.15	~ 1000λ
I_{33}	50λ 700°C, 10 sec 250λ 600°C, 15 sec	9.615	8.915	107.73	144.03	~ 300λ
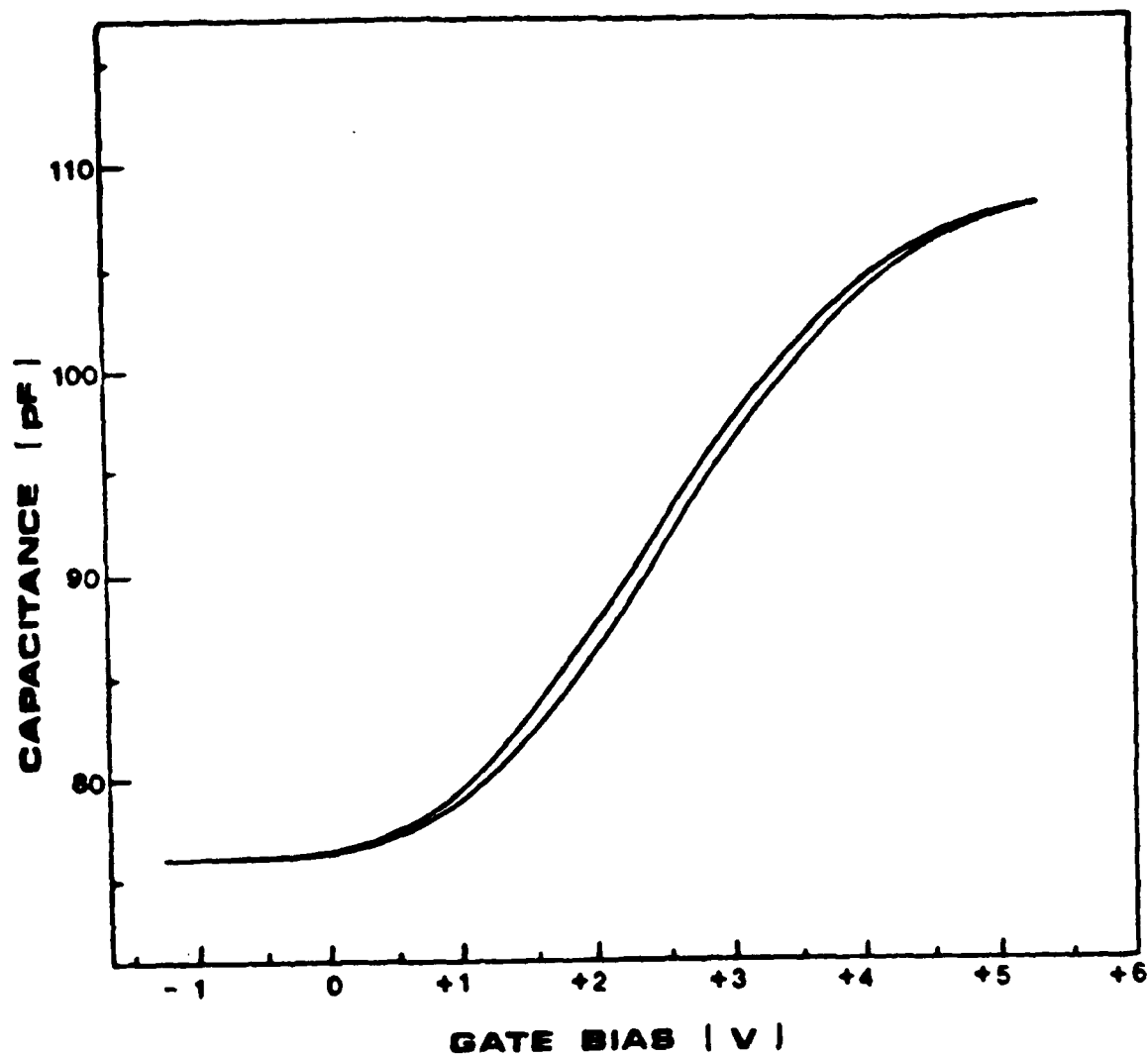
Fig. 11   Capacitance-Voltage Characteristics of Epitaxial CaF_2 on InF.

SIMULATION OF SELF-ALIGNED GATE PROCESSING FOR INDIUM PHOSPHIDE MISFETS

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51

SIMULATION OF SELF-ALIGNED GATE PROCESSING
FOR INDIUM PHOSPHIDE MISFETS

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CINCINNATI, OHIO   45221

MIKE BIEDENBENDER
GREG JOHNSON
MOHSEN SHOKRANI

INTRODUCTION

1   P - DOPED SILICON DIOXIDE THIN FILM
    AS AN ENCAPSULANT AND GATE DIELECTRIC

2   ION IMPLANTATION AND THERMAL
    ANNEALING OF THIN FILMS

3   InP MISFET FABRICATION

SAMPLE PREPARATION

InP SUBSTRATES: N-TYPE (Sn),(100),1×10^{16} cm^{-3}

SEMI-INSULATING (FE),(100),$R=1E7\Omega$-CM

CLEANING PROCEDURES:
STANDARD DEGREASE

INITIAL CLEANING

30 sec - (1:1:4)12:1 (HCl:HF:H_2O):H_2O_2

30 sec - 10% H_3PO_4/H_2O

5 min - DI WATER RINSE

3 min - 10 wt% HIO_3/H_2O

5 min - DI WATER RINSE

15 sec - (1:1:4)12:1 (HCl:HF:H_2O):H_2O_2

15 sec - 10% H_3PO_4/H_2O

5 min - DI WATER RINSE

N_2 BLOW DRY

PRIOR TO INSULATOR DEPOSITION

15 sec - 10:1 H_2O:HF

5 min - DI WATER RINSE

N_2 BLOW DRY

OHMIC CONTACT: MIS CAPACITOR BACK CONTACT

Au/Ge 12% EUTECTIC (1500Å): Au (1000Å)

ALLOY 5 MIN, 400 C, 10% H_2/N_2 1000 SCCM

SiO_2 FILM DEPOSITION

TECHNICS PLANARETCH PEII-A   13.56 MHz/
AUTOMATIC MATCHING

PROCEDURE:
1. CHAMBER ETCH $\quad\quad$ CF_4, 150W, 25 MIN
2. N_2 PLASMA CLEAN $\quad\quad$ N_2, 100W, 5 MIN
3. BAKEOUT $\quad\quad\quad\quad\quad$ N_2, 5 MIN, 275 C
4. LOAD SUBSTRATES AND P_4 SOURCE
5. BAKEOUT $\quad\quad\quad\quad\quad$ N_2, 2 HOURS, 275 C
6. INTRODUCE REACTANTS
7. DEPOSIT

PHOSPHORUS RICH INTERFACE

1. N_2 PLASMA   5MIN, 30W, 275C, 20 SCCM, 500mTORR
2. N_2O PLASMA   1MIN, 30W, 275C, 30 SCCM, 500mTORR

SiO_2
1. 800 mTORR, 30 WATT RF
2. 275 C SUBSTRATE TEMPERATURE
3. N_2O; 55SCCM, SiH_4; 17.4SCCM

RAPID THERMAL ANNEALING
(SiO_2 FILMS AS ENCAPSULANT AND GATE)

SYSTEM: PROCESS PRODUCTS CORP.
RAPID HEAT MODUAL

H_2 RTA:

1. 700 C
2. 30 SEC
3. H_2 FLOW RATE = 2 LITER/MIN

N_2 RTA:

1. 700 C
2. 30 SEC
3. N_2 FLOW RATE = 2 LITER/MIN

LOW TEMPERATURE FURNACE ANNEAL
1. 1 HOUR
2. 400 C
3. 10% H_2/N_2 FLOW RATE = 1 LITER/MIN

THERMAL PROCESSING OF INSULATORS

"AS DEPOSITED"

LOW TEMPERATURE ANNEAL

H_2 RTA

N$_2$ RTA

1) H_2 RTA
2) LOW TEMPERATURE ANNEAL

1) N_2 RTA
2) LOW TEMPERATURE ANNEAL
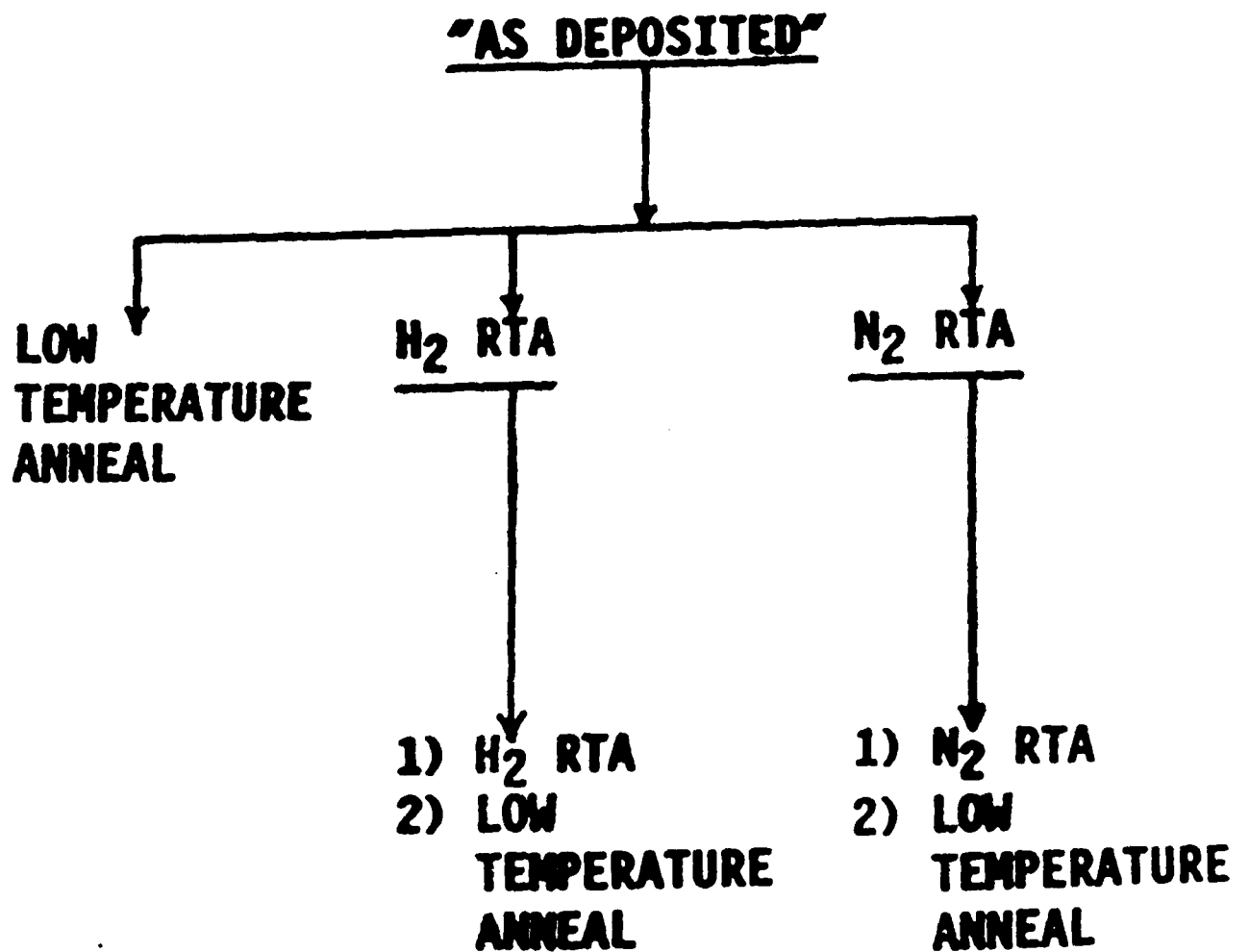
AES ANALYSIS OF SiO$_2$ (WITH PHOSPHORUS)

In(MNN)

P(LMM)

O(KLL)

Si(KLL)

$\frac{dN(E)}{dE}$ PEAK TO PEAK HEIGHT (au)

SPUTTER TIME (min)
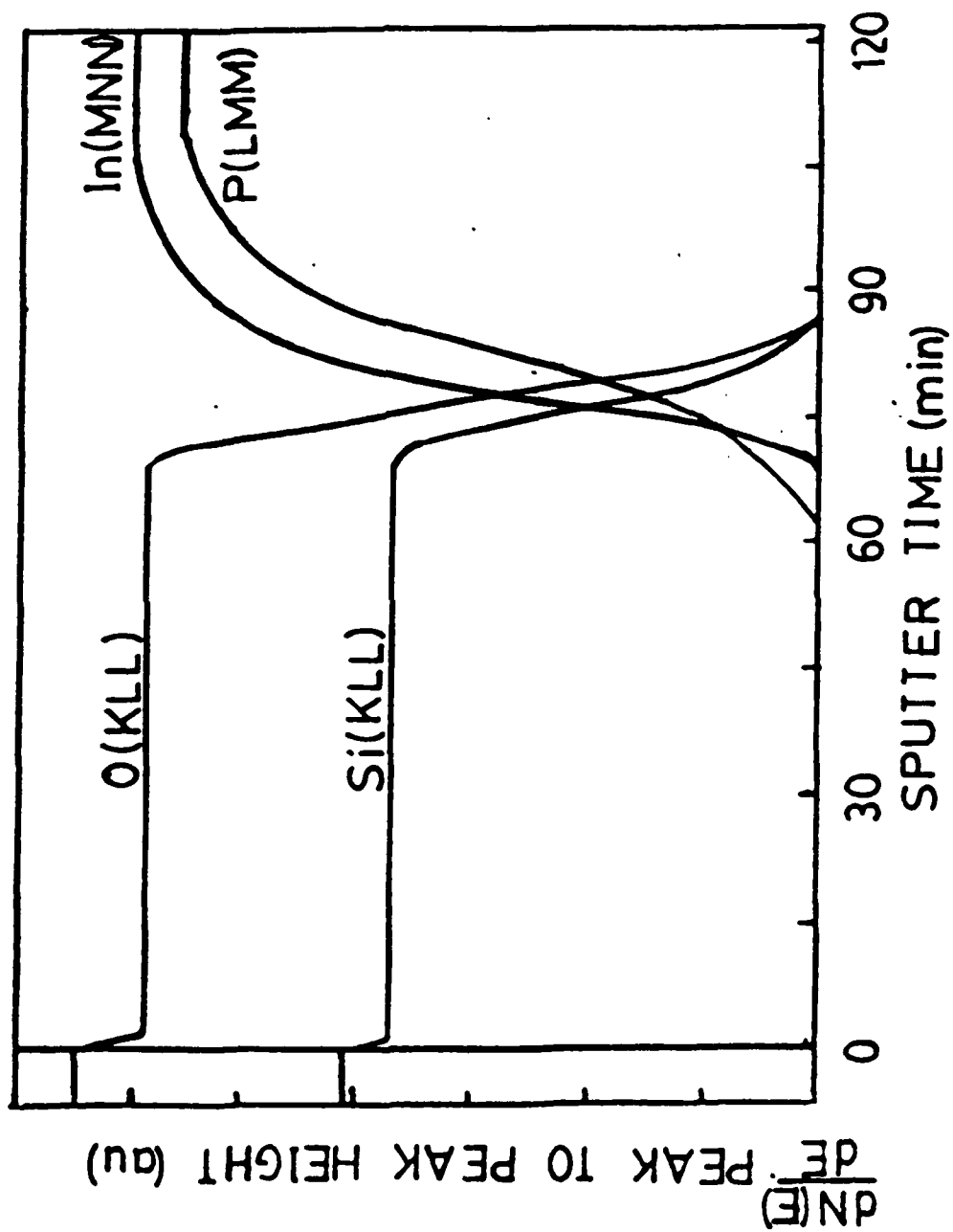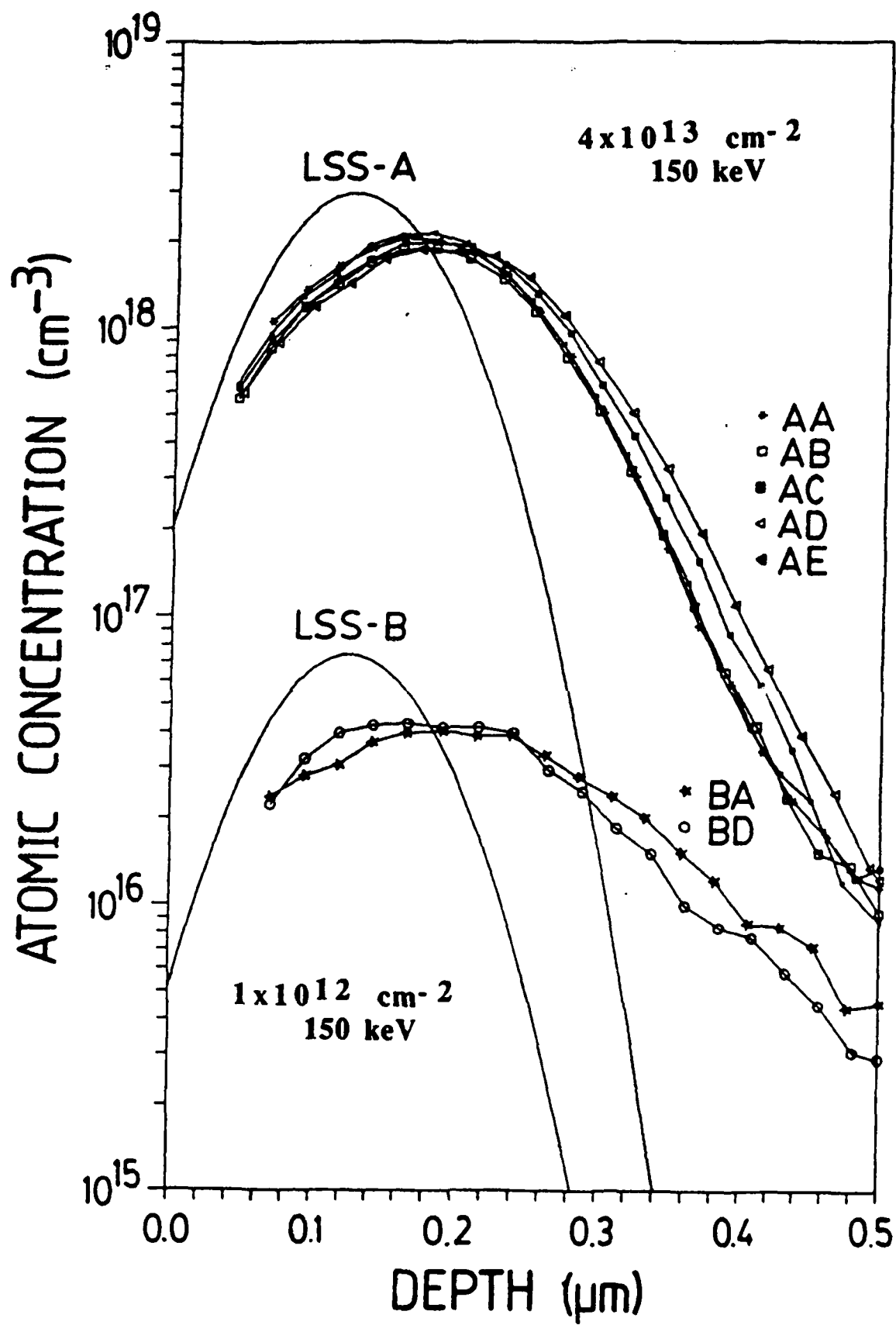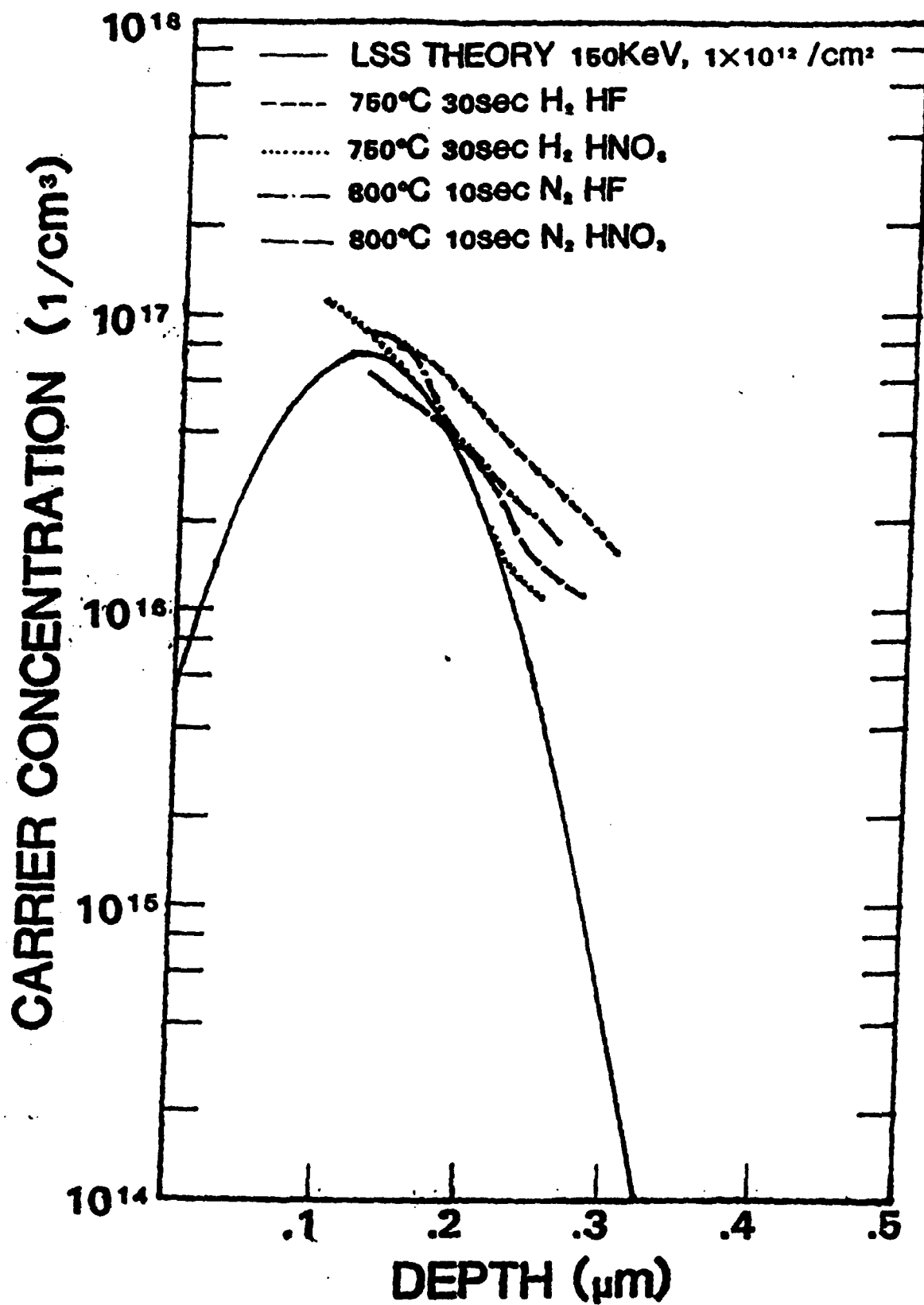
ELECTRON CONCENTRATION PROFILES

InP MISFET FABRICATION

. INITIAL CLEAN

. ALIGNMENT MARKS
  -(MASK #1)
  -ETCH 1000Å InP:
   10wt% HIO_3/H_2O
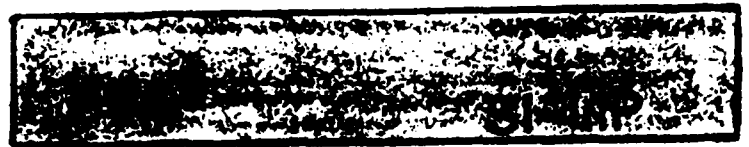
. SOURCE/DRAIN
  IMPLANTATION
  -(MASK #2)
  -DEGREASE
  -30 sec 1:1 H_2O:HF
  -PHOTORESIST IMPLANT
   MASK
  -Si: 150keV, $4\times10^{13}cm^{-2}$
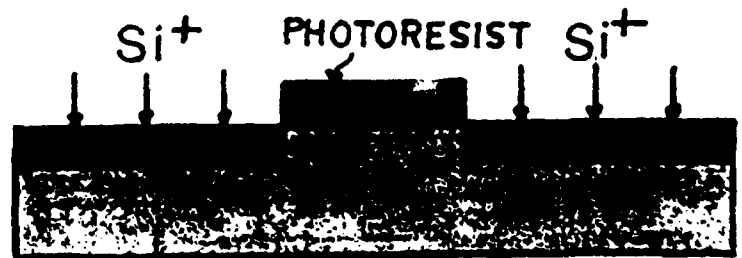
INSULATOR DEPOSITION
-DEGREASE
-30 sec 1:1 H_2O:HF
-SiO_2: 275 C, 30W, 800mTORR, 1000A

InP MISFET FABRICATION

. RAPID THERMAL
ANNEAL
-700 C FOR 30SEC
-H_2 OR N_2
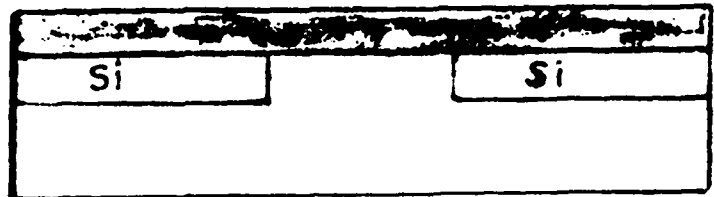
. SOURCE/DRAIN CONTACTS
-(MASK #3)
-Au/Ge 12 wt% (1500Å)
-Au (1000a)
-LIFT-OFF PROCESS
-ALLOY CONTACTS

AU/GE:AU
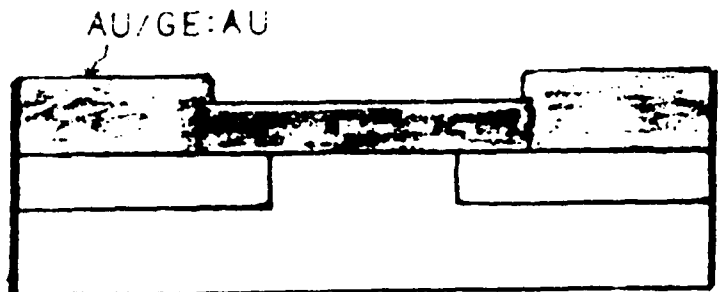
GATE METALIZATION
-(MASK #6)
-Ti (500Å)
-Au (4000Å)
-LIFT OFF PROCESS
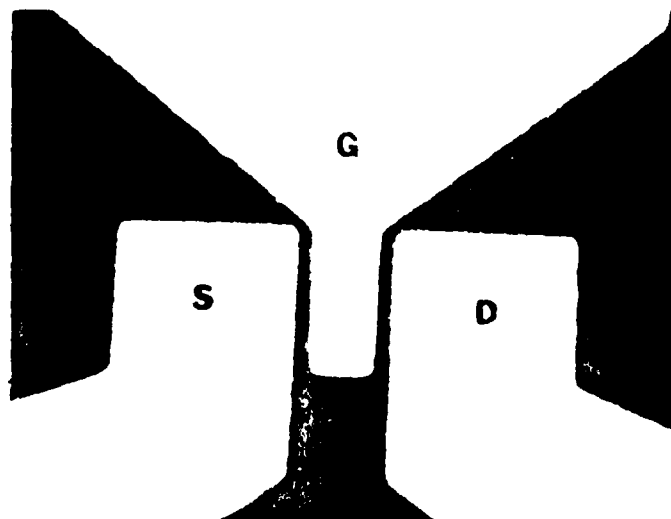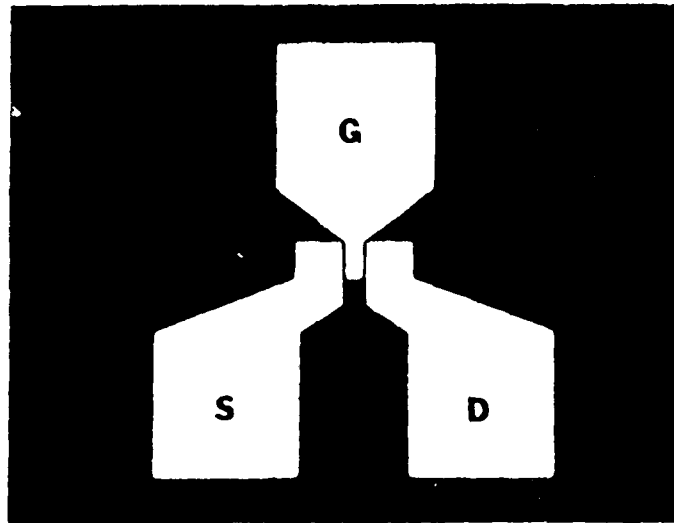
T:AU

In P. MISFET

InP MISFET I-V CHARACTERISTICS

SiO.
N.
RTA

$V_t = 1.25v$

$u = 600 \, cm^2/v\text{-}s$

mA

SiO
N
RTA

LOW
TEMP
ANL

$V_t = 1.5v$

$u = 600 \, cm^2/v\text{-}s$

mA
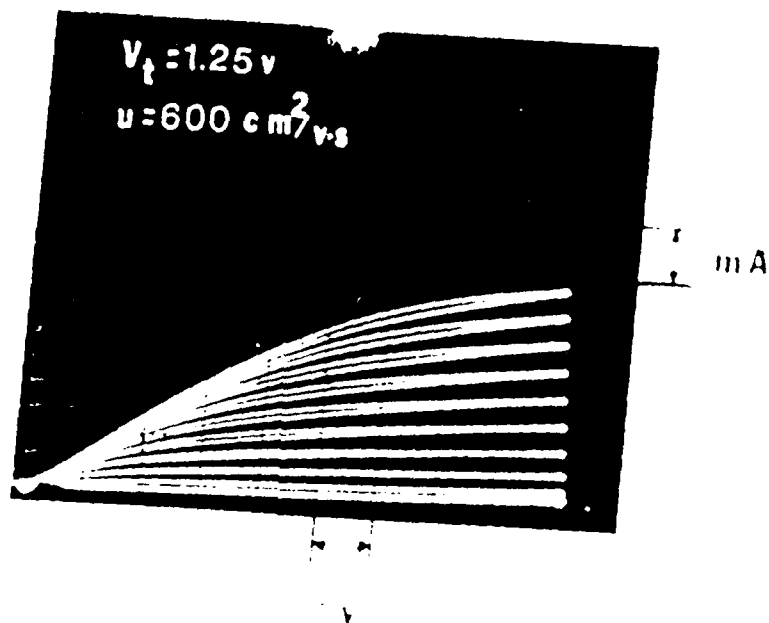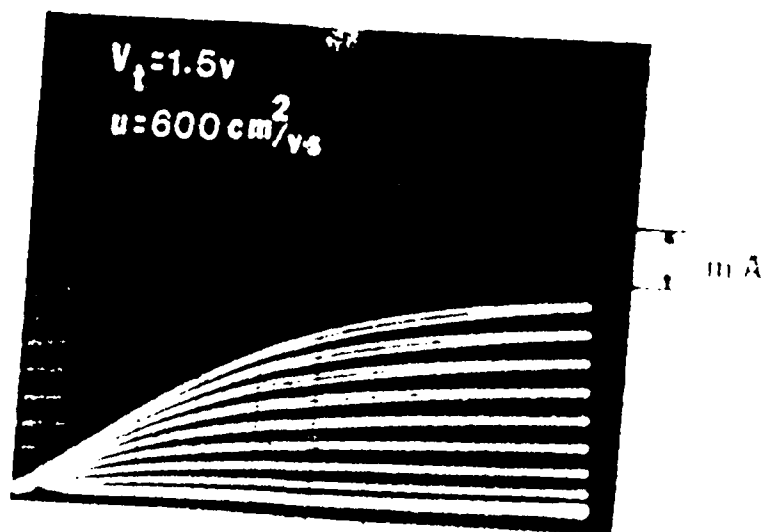
InP MISFET I-V, CHARACTERISTIC

SiO₂
H₂
RTA

$V_t = 6 v$

$u = 20 \, cm^2/v \cdot s$

50 ₊ A

1 v

SiO₂
H₂
RTA

LOW
TEMP
ANL

$V_t = 1.5 v$

$u = 1200 \, cm^2/v \cdot s$

$D_{it} = 3 \cdot 10^{11}/cm^2 \cdot eV$

1 m A

1. v

.5 m A
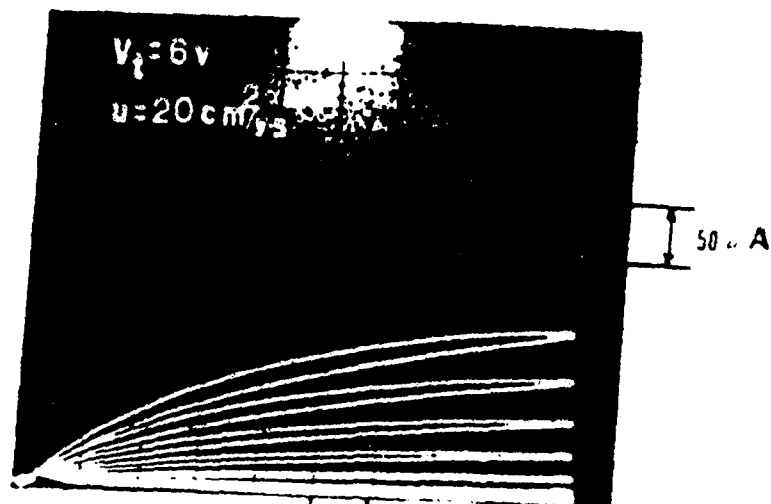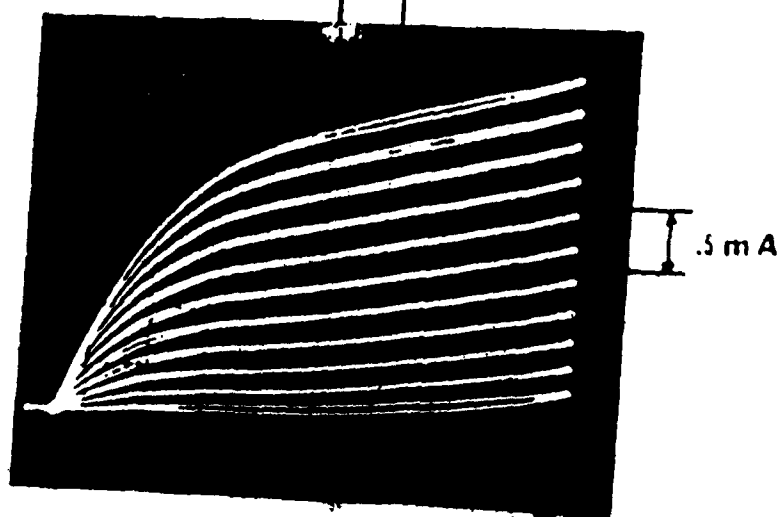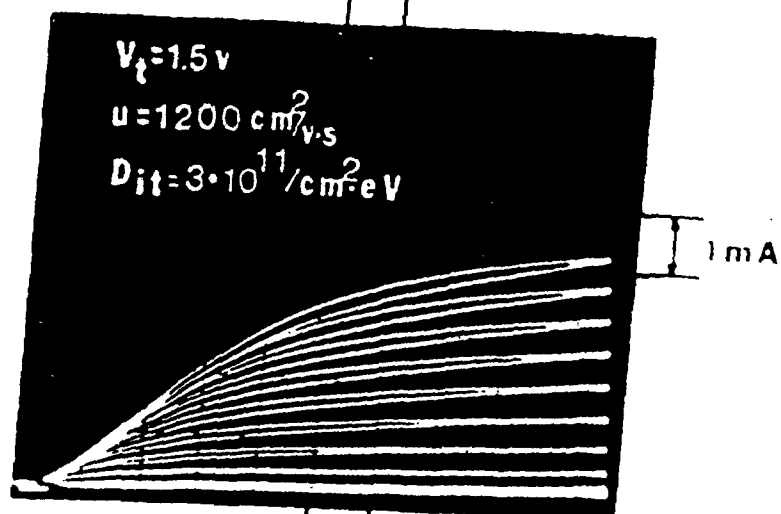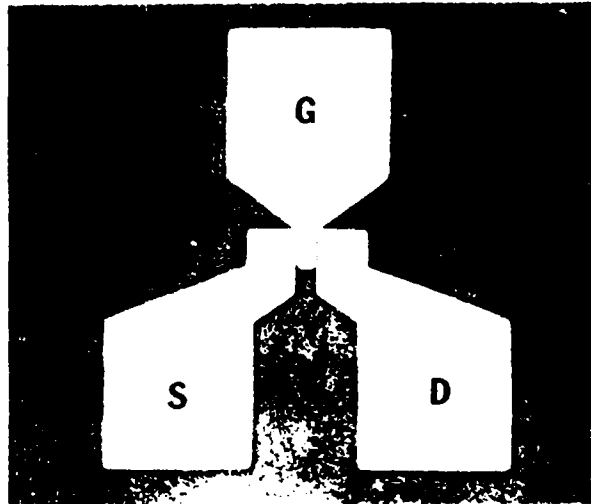
InP MISFET

I - V CHARACTERISTICS
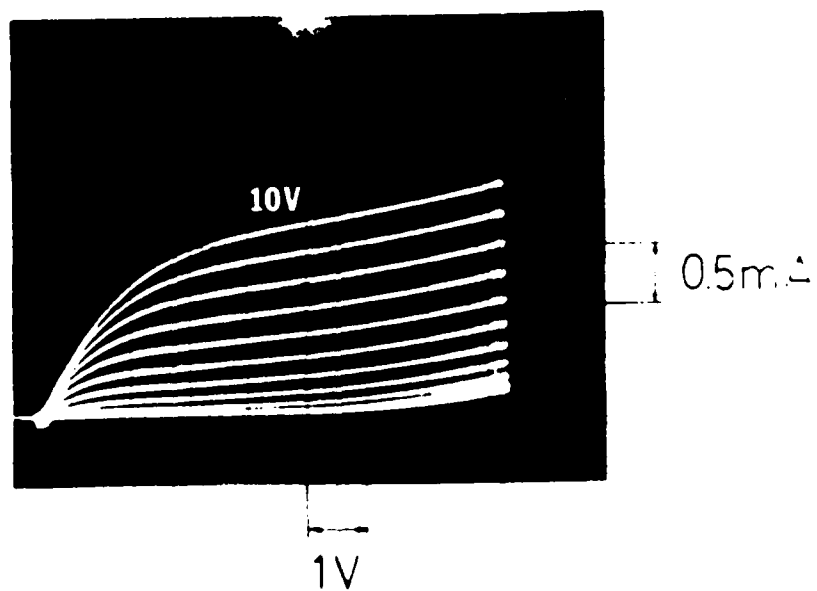
I - V
cuive for
InP MISFET
with a
Ge_3N_4 Insulator
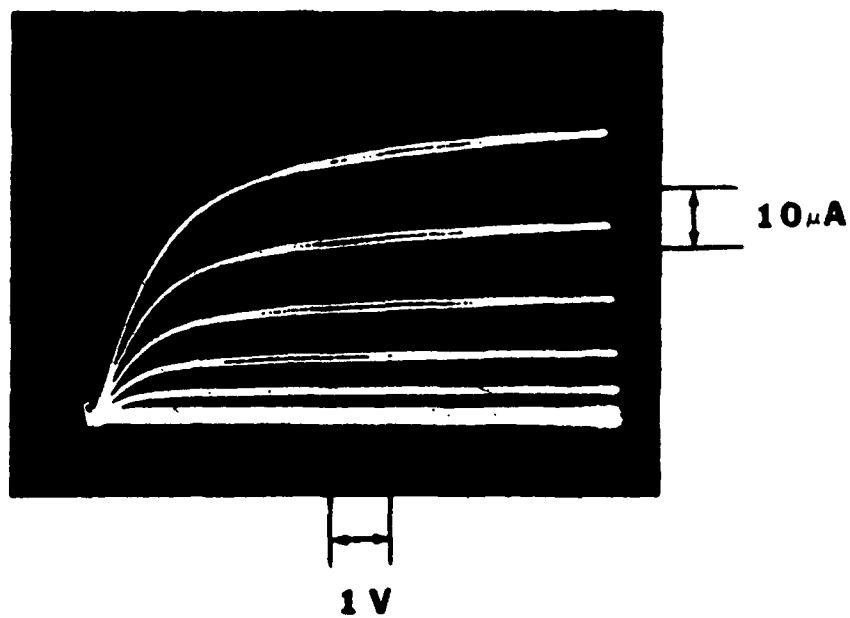
10μA

1 V

PHOTOLUMINESCENCE AS A TECHNIQUE FOR ASSESSING THERMAL DAMAGE AND
IMPLANT ACTIVATION DURING POST-IMPLANT ANNEAL OF Si-IMPLANTED InP

R. R. Chang and D. L. Lile

Colorado State University
Fort Collins, CO
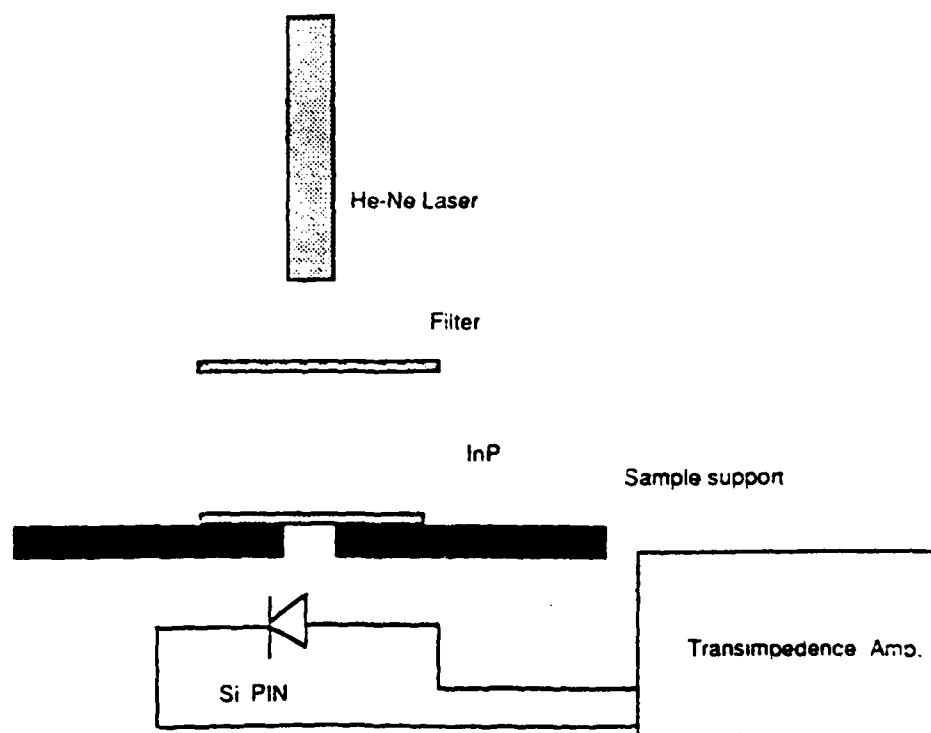
Fig.4.6 Schematic illustration of the apparatus employed for
photoluminescence measurements ex situ.

Photoluminescence (arbitrary units) vs Doping Density (cm⁻³)
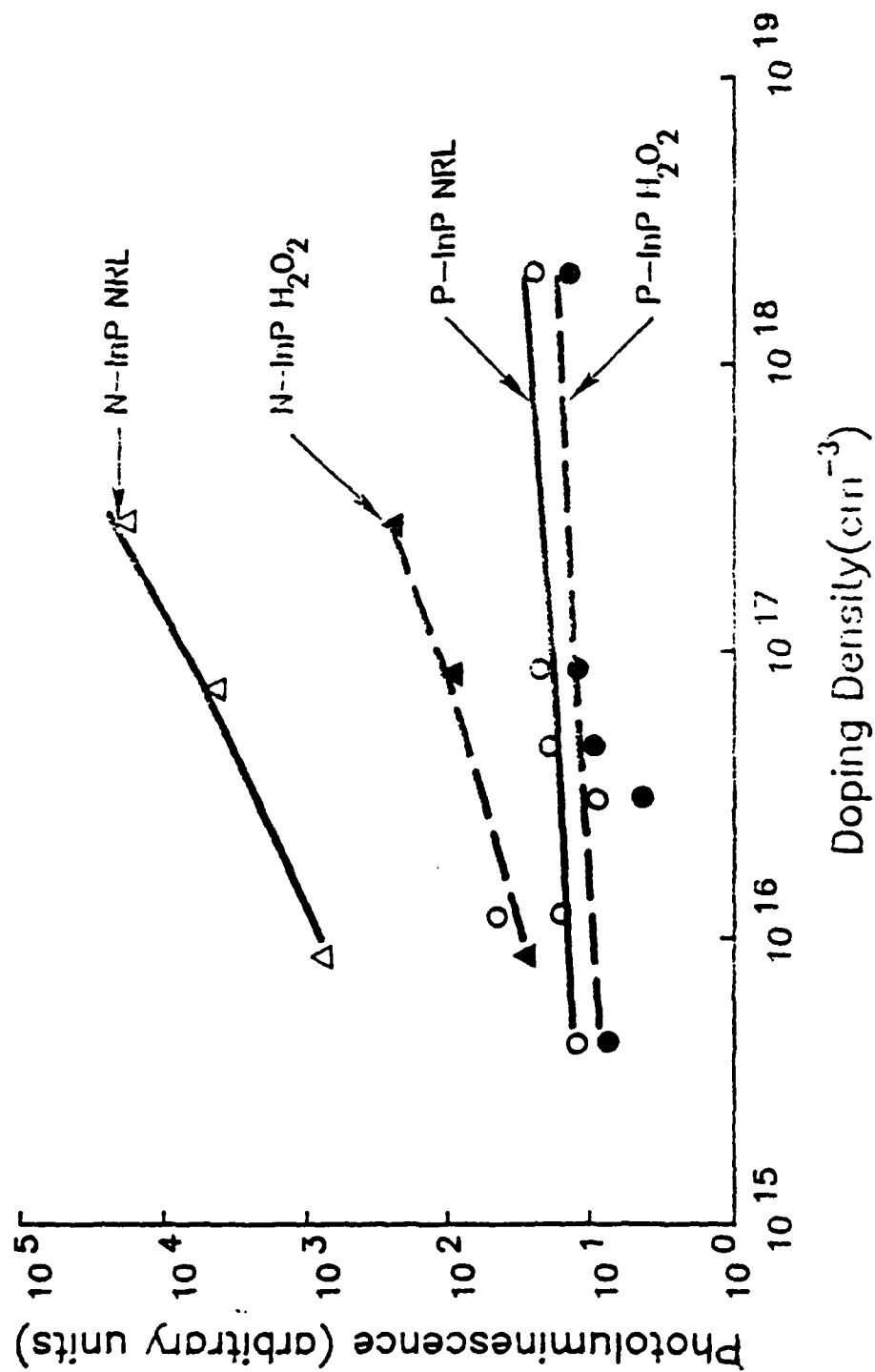
Ion Implantation

- Nonactive Impurities
- Crystal Damage

Thermal Annealing

- Activates Impurities ⟶ Increased PL
- Recrystallize Lattice ⟶ Increased PL
- Causes Thermal Degradation ⟶ Reduced PL

800°C RTA

(b)

(a)

Annealing time(sec)

74

5 μec RTA.

Photoluminescence (arbitrary units)

Annealing temperature (C)

Capped with SiO₂ & red phosphorous (c)

SiO₂ (b)

Capless (a)

Original PL

75
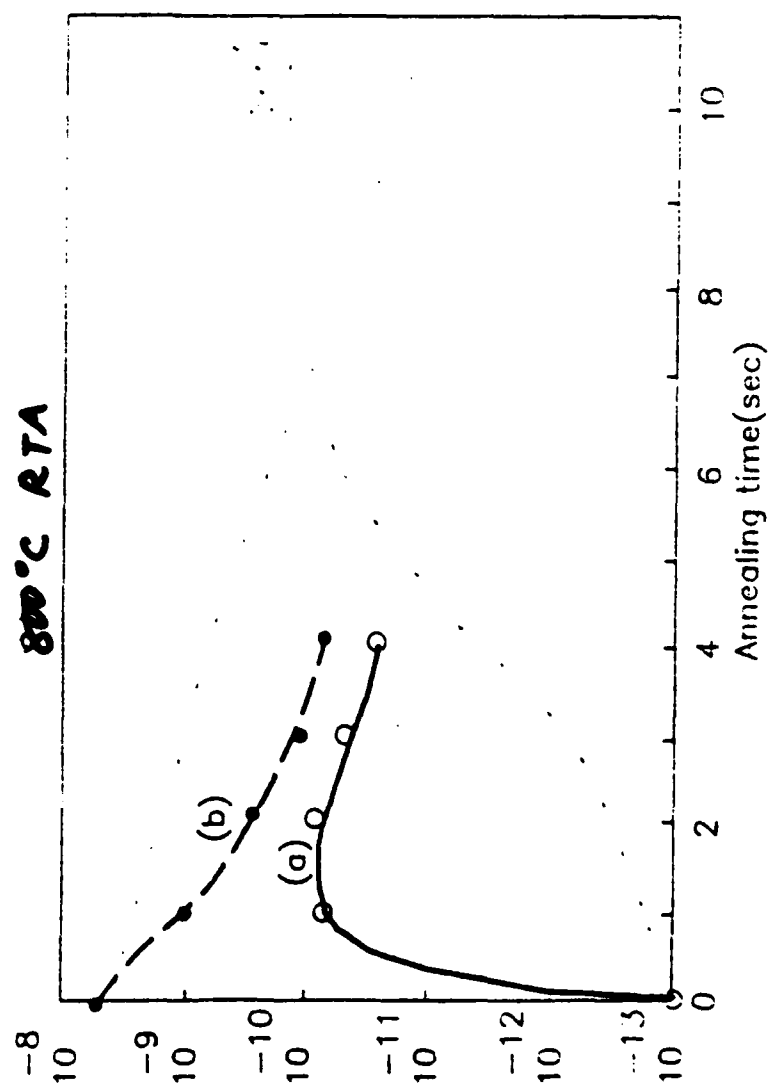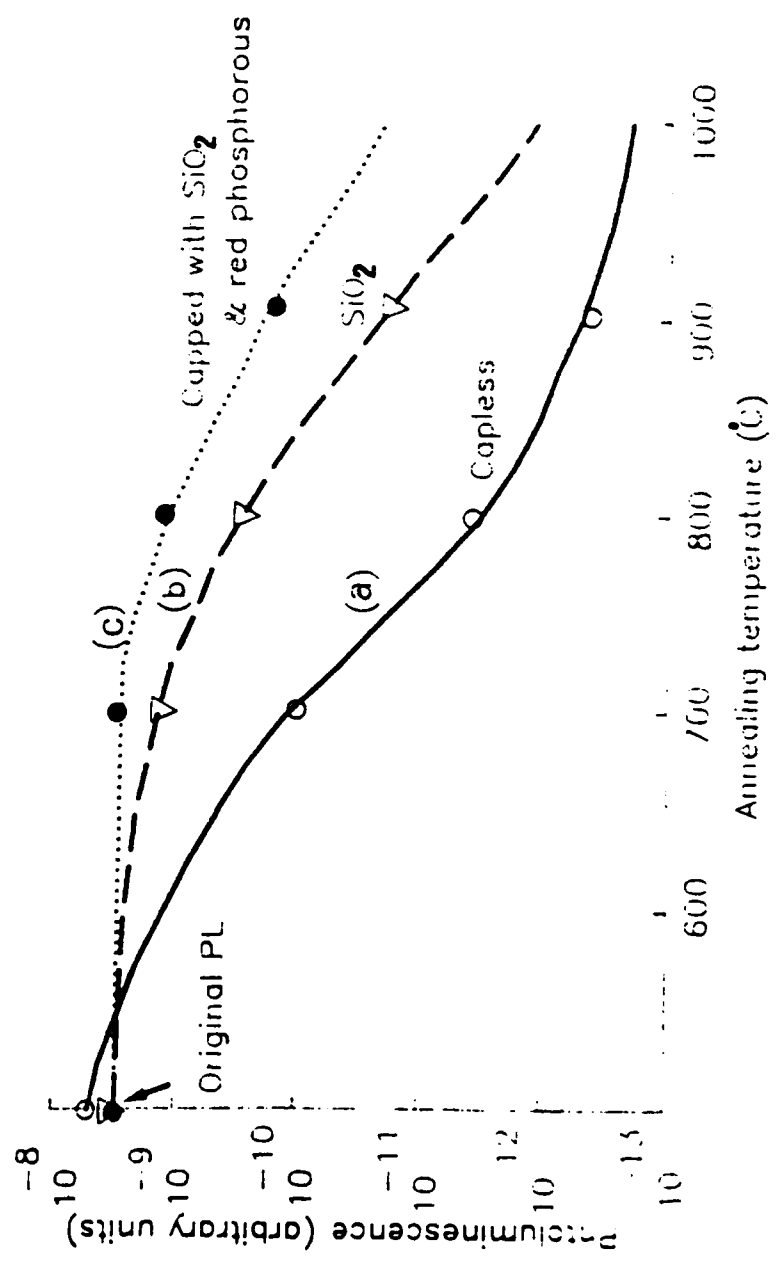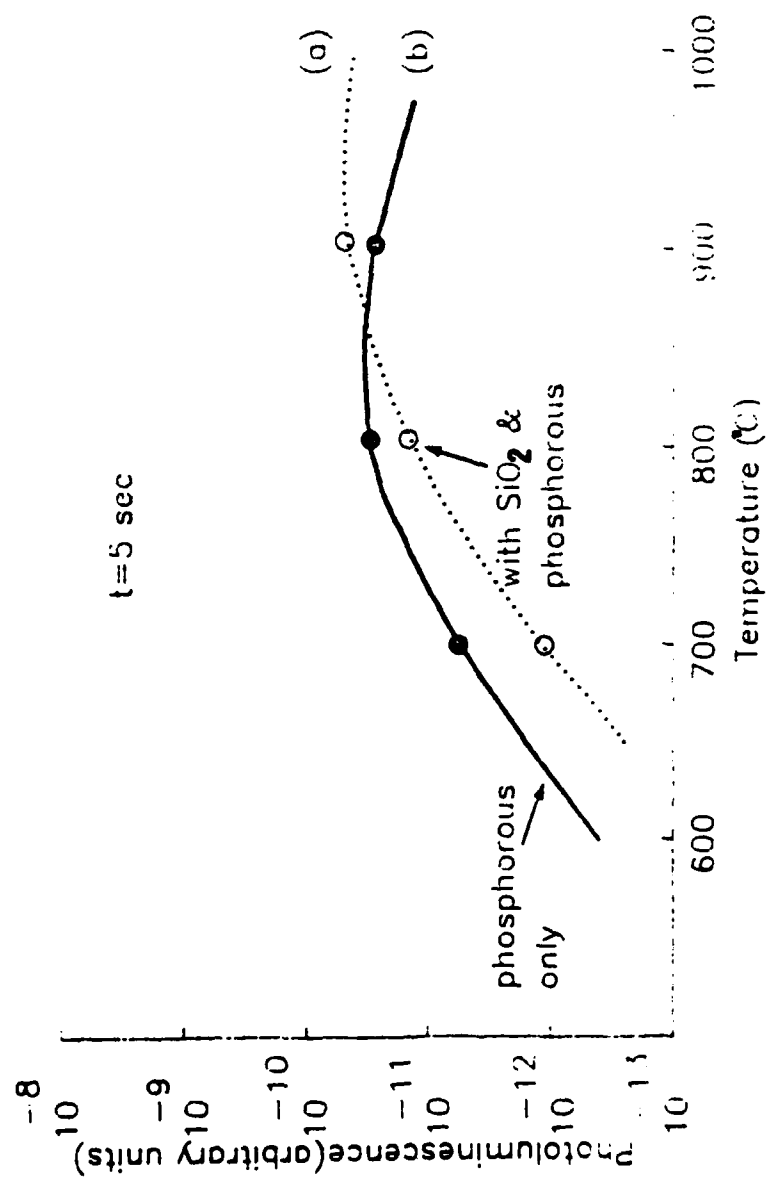
Fig.5.17 *Variation of the photoluminescence response with annealing temperature for a constant annealing time of 5 seconds. Annealing was performed with an overpressure of phosphorous on an implanted Si-Ini sample(a), with a 2000 Å SiO₂ cap and, (b), without a cap.*
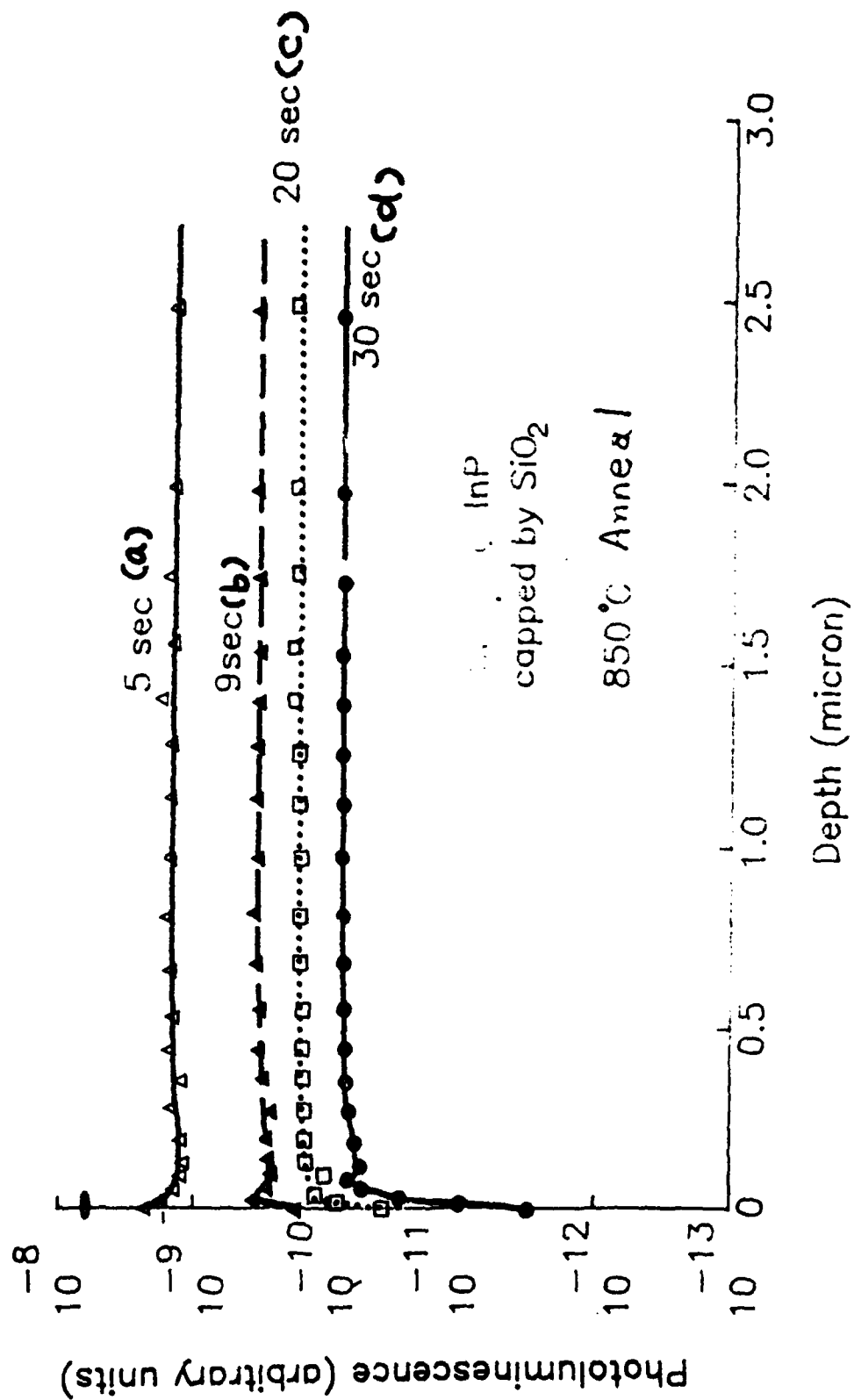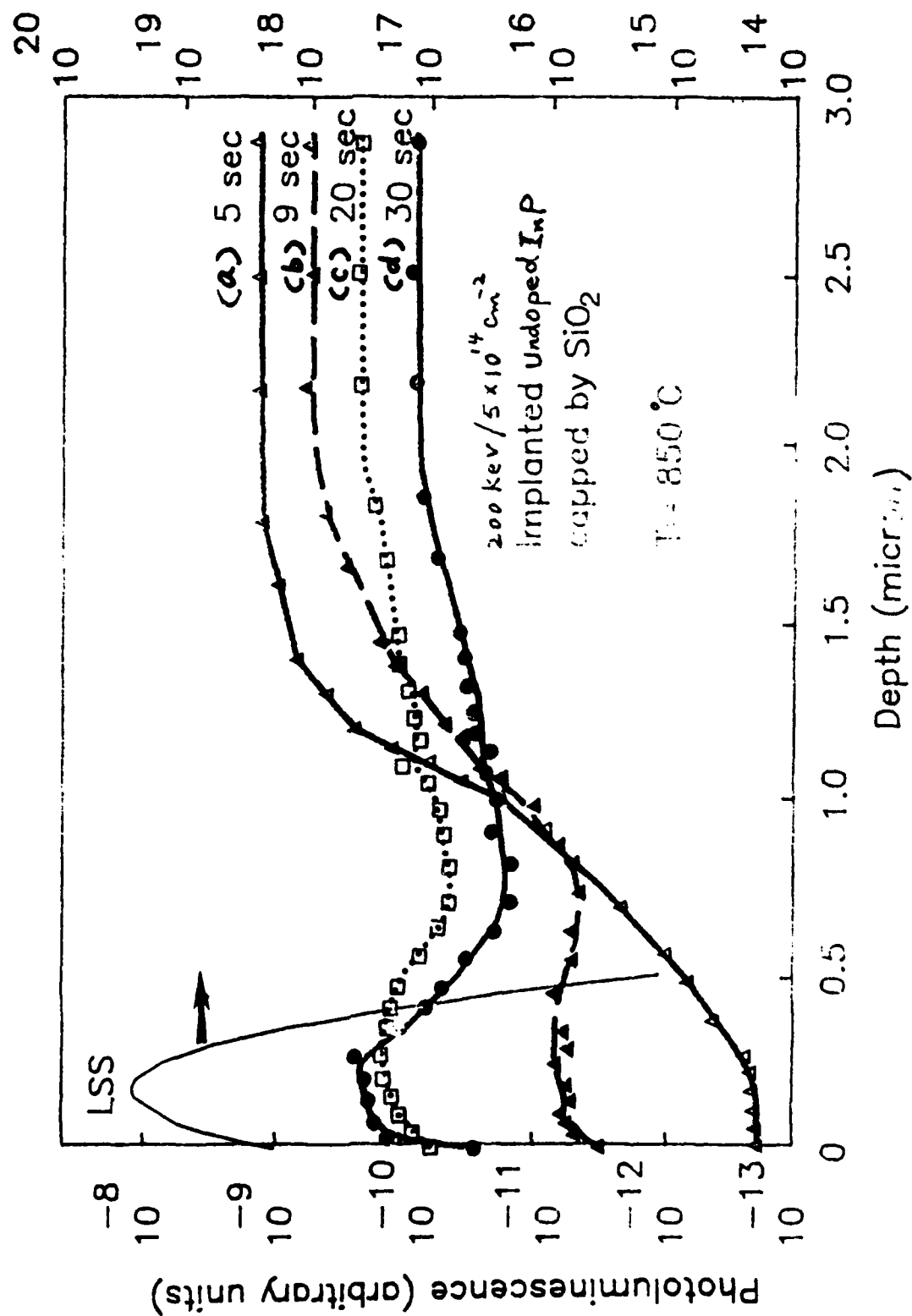
Photoluminescence (arbitrary units)

Depth (micron)

5 sec (a)

9 sec (b)

20 sec (c)

30 sec (d)

InP
capped by SiO_2

850°C Anneal

-7-

Photoluminescence (arbitrary units)

Depth (micron)

LSS

(a) 5 sec
(b) 9 sec
(c) 20 sec
(d) 30 sec

200 keV/5×10^{14} cm^{-2}
implanted undoped InP
capped by SiO$_2$

T = 850°C

P/N JUNCTION VAPOR PHASE EPITAXIAL GROWTH IN InP and InP JFET RESULTS WITH ALL EPITAXIAL LAYER GROWTH

J. Crowley, D. Tringali and B. Fank

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"P/N JUNCTION VAPOR PHASE EPITAXIAL GROWTH IN InP AND InP JFET RESULTS WITH ALL EPITAXIAL LAYER GROWTH"

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High quality epitaxial growth of N-type doped InP crystal using vapor phase techniques has been well established for some time. However, the sequencial epitaxial growth of P-type and N-type doping layers in InP has not been well demonstrated, especially using vapor phase techniques. Since device designs with both P and N layers in InP have excellent potential, (specifically millimeter wave JFets and Impatts) work was undertaken to make a special VPE reactor with this growth capability. This paper describes the reactor design used to achieve the high quality P/N epitaxial junction and its application to the development of an all epitaxial InP JFet.

Using a two chamber design with separate N-type (sulfur dopant) and P-type (zinc dopant) doping chambers, excellent P/N junctions have been grown in InP. Polaron measured doping profiles show short transitions from N-type doping in the low $10^{17}/cm^3$ range to P-type doping in the mid $10^{19}/cm^3$ range. Some initial SIMS measurements show both "clean" junctions and some possible zinc penetration into the N sulfur doped region. Some rationale for both of these conditions can be given.

With this P/N junction growth capability established, wafers with doping profiles for InP JFets have been grown. Fabrication techniques have been developed for the JFet and a number of devices have been made and tested. Results to date of a JFET with a complete epitaxial design and construction show a measured transconductance of 50 ms/mm with a 2.7 um gate length. A number of design and fabrication changes are being made to improve the performance to expected levels for an InP FET.

JC006

InP JFET DEVELOPMENT

* GOALS AND OBJECTIVES

* MATERIAL GROWTH AND CHARACTERIZATION

* DEVICE FABRICATION

* ELECTRICAL EVALUATION

* CONCLUSIONS

InP JFET DEVELOPMENT

GOALS

* EPITAXIAL InP P/N JUNCTION
* POWER InP JFET
    Po/Z > 1.5 W/mm @ 20GHz

OBJECTIVES

* DEVELOP VPE REACTOR WITH BOTH P-TYPE
    AND N-TYPE DOPING CAPABILITY
* CHARACTERIZE MATERIAL
* OPTIMIZE EPI STRUCTURE FOR JFETs
* ESTABLISH FABRICATION PROCESS
* PERFORM DC AND RF EVALUATION
* MODEL DEVICE

InP VPE REACTOR
P-Type and N-Type Doping

H₂+PCl₃

VE Line   H₂+PCl₃

DE2

Split
Chamber
Liner

Vent

Front View
Split Chamber Liner

In+H₂S

750°C

670°C

FURNACE PROFILE

84
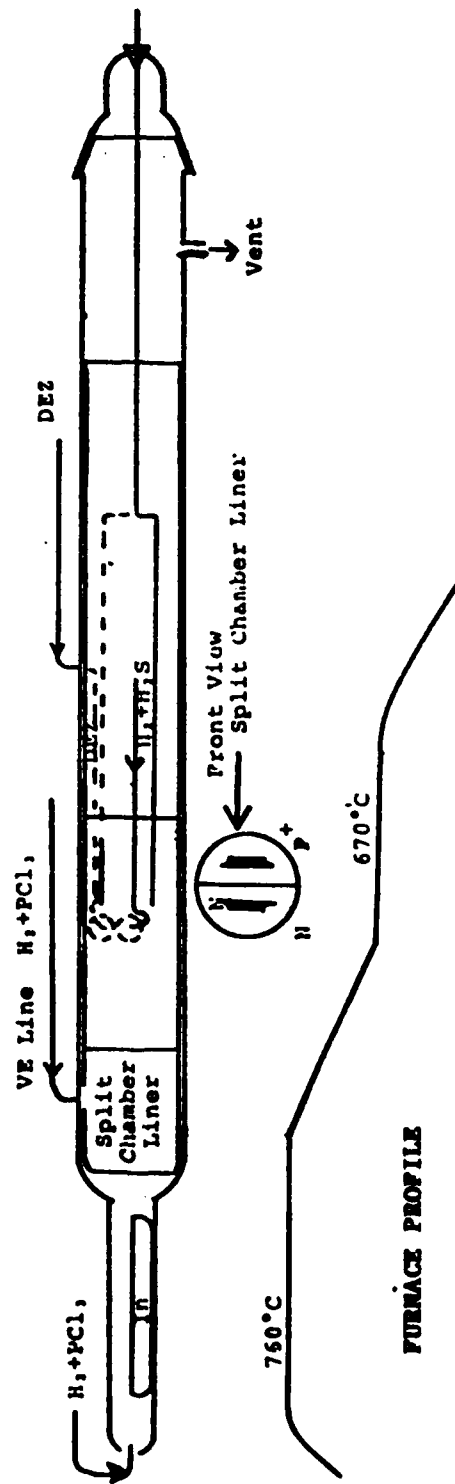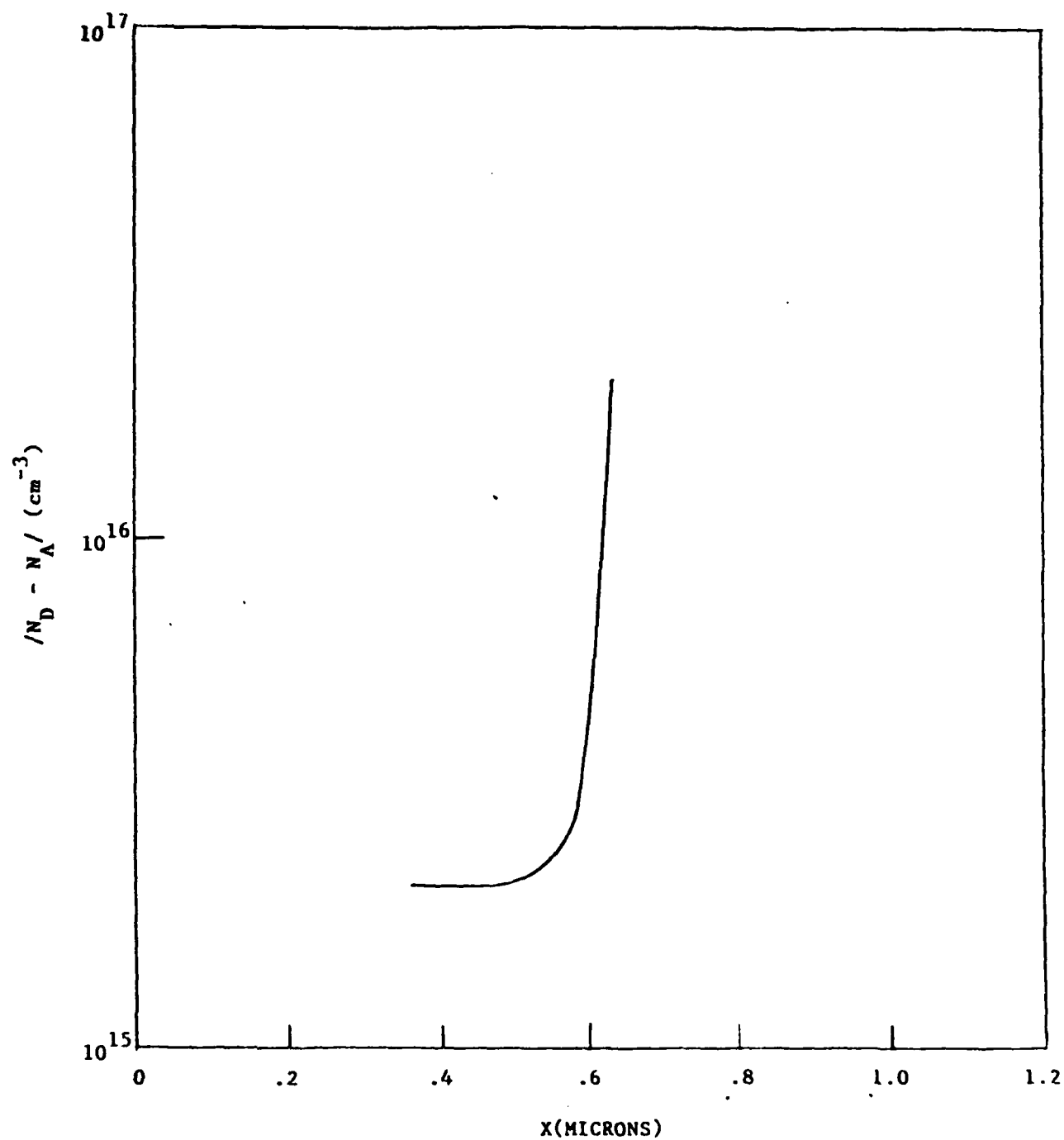
Measured Transition Between Two Epi Layers
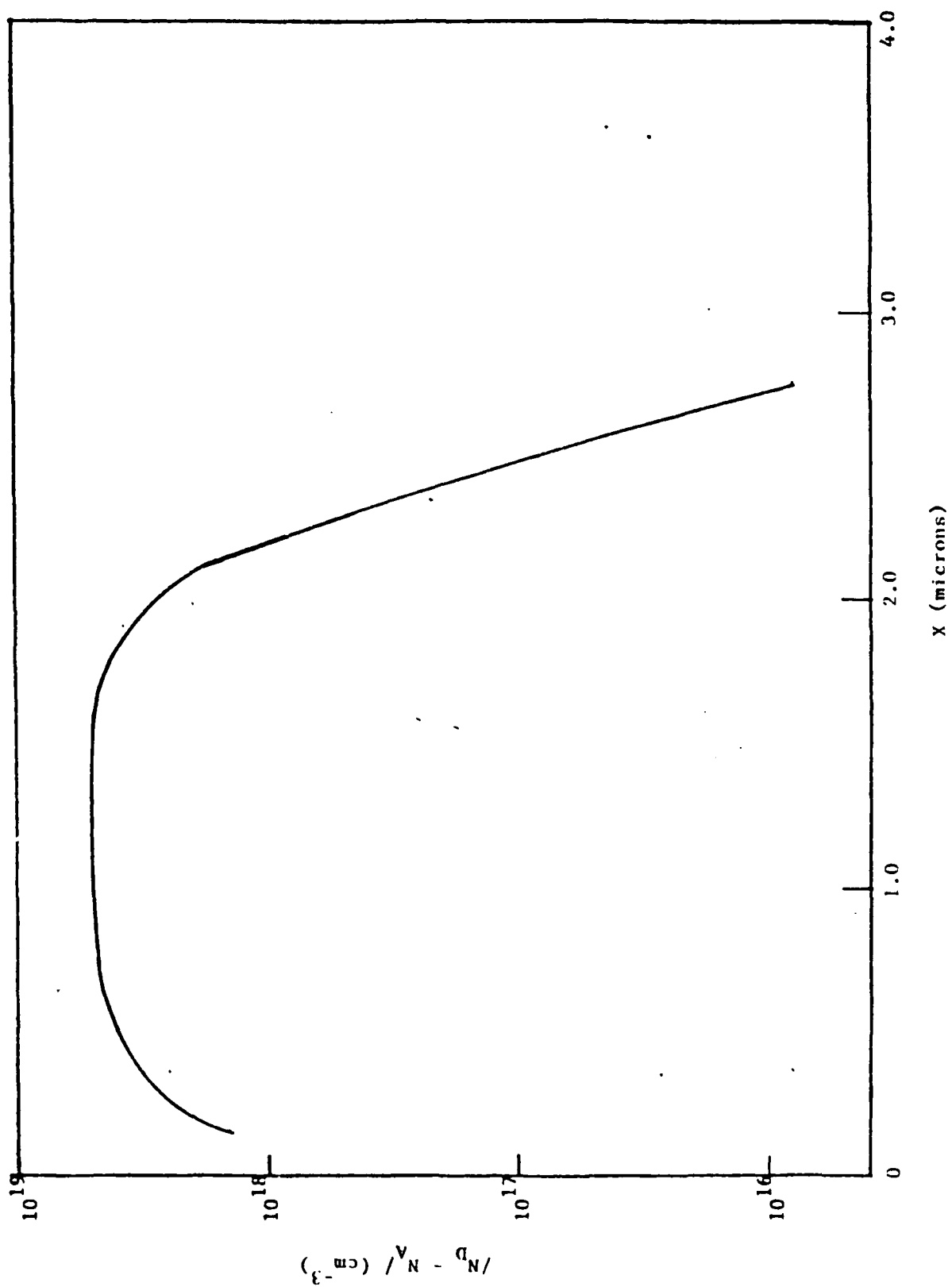
Typical Measured P-Type Doping Profile

$/N_D - N_A/ \ (cm^{-3})$

P$^+$ gate	1.6e 18	0.59
N channel	3.4e 17	0.51

semi-I (100) Fe -3deg sub # cc 3286

X (microns)
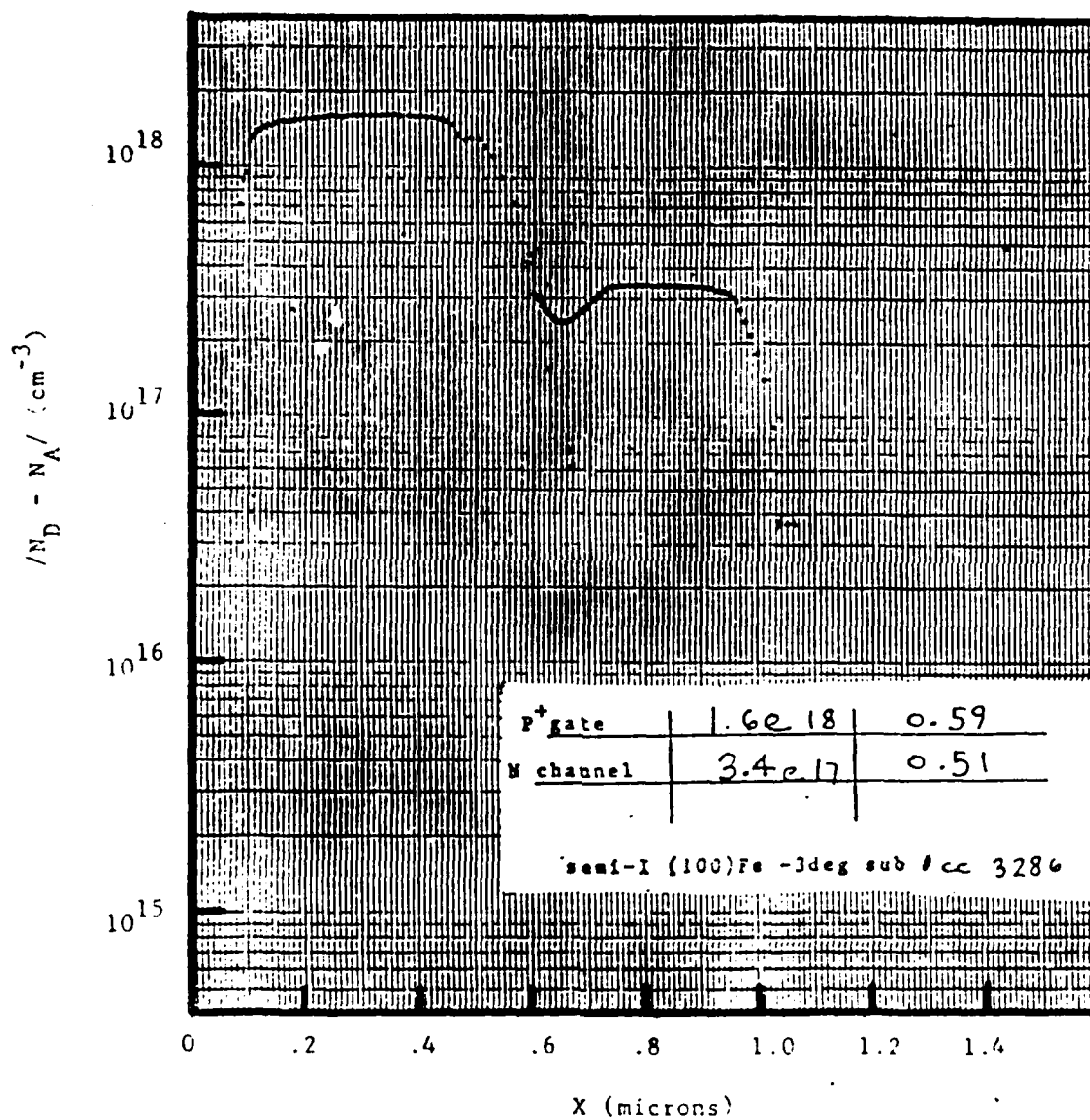
Measured Doping Profile of JFET Wafer IPJ 3-2
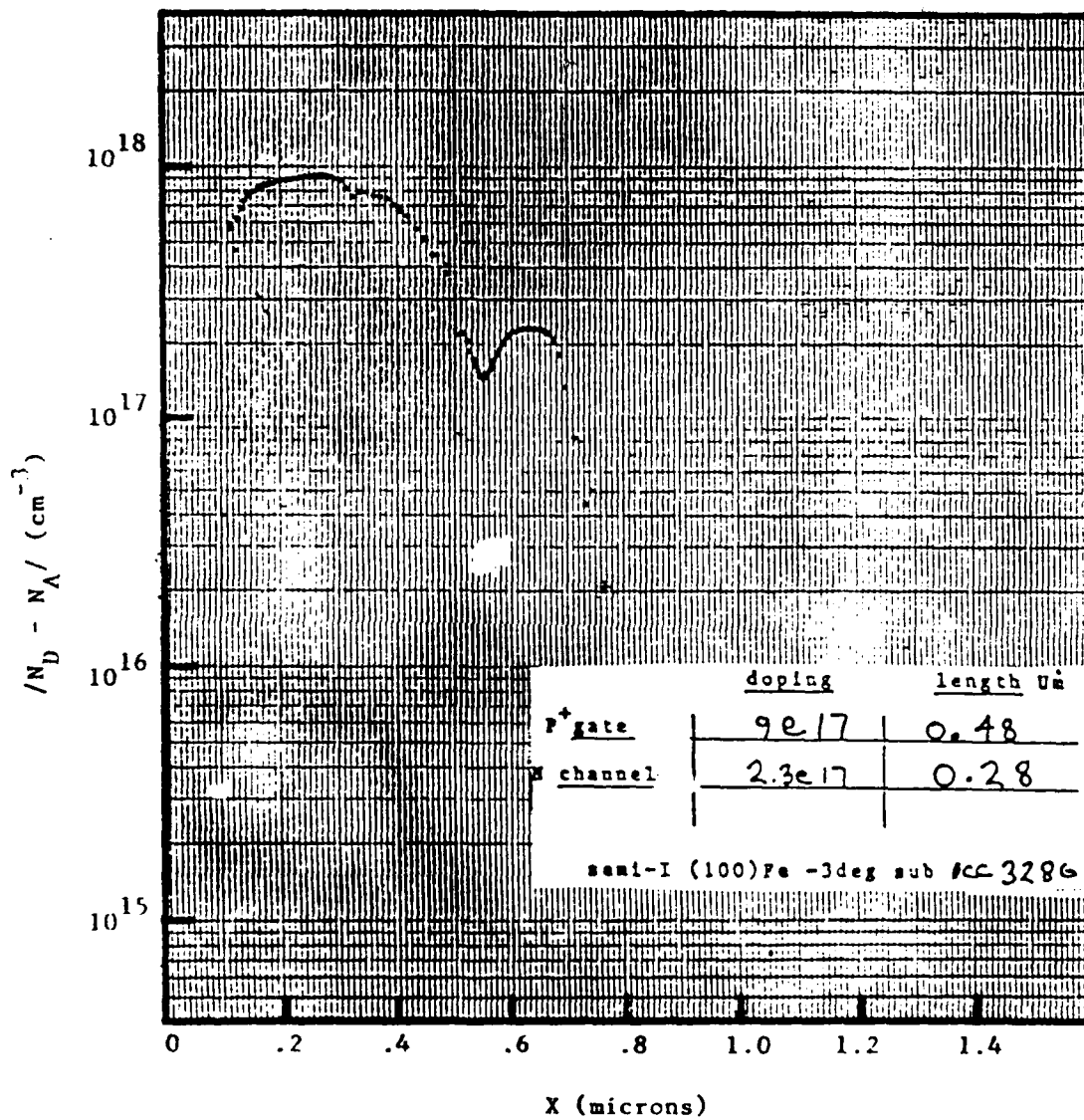
Measured Doping Profile of JFET Wafer IPJ 3-1

C-V DATA FOR IPJ0409

V (VOLTS)

1/C^2 (1/pF^2)
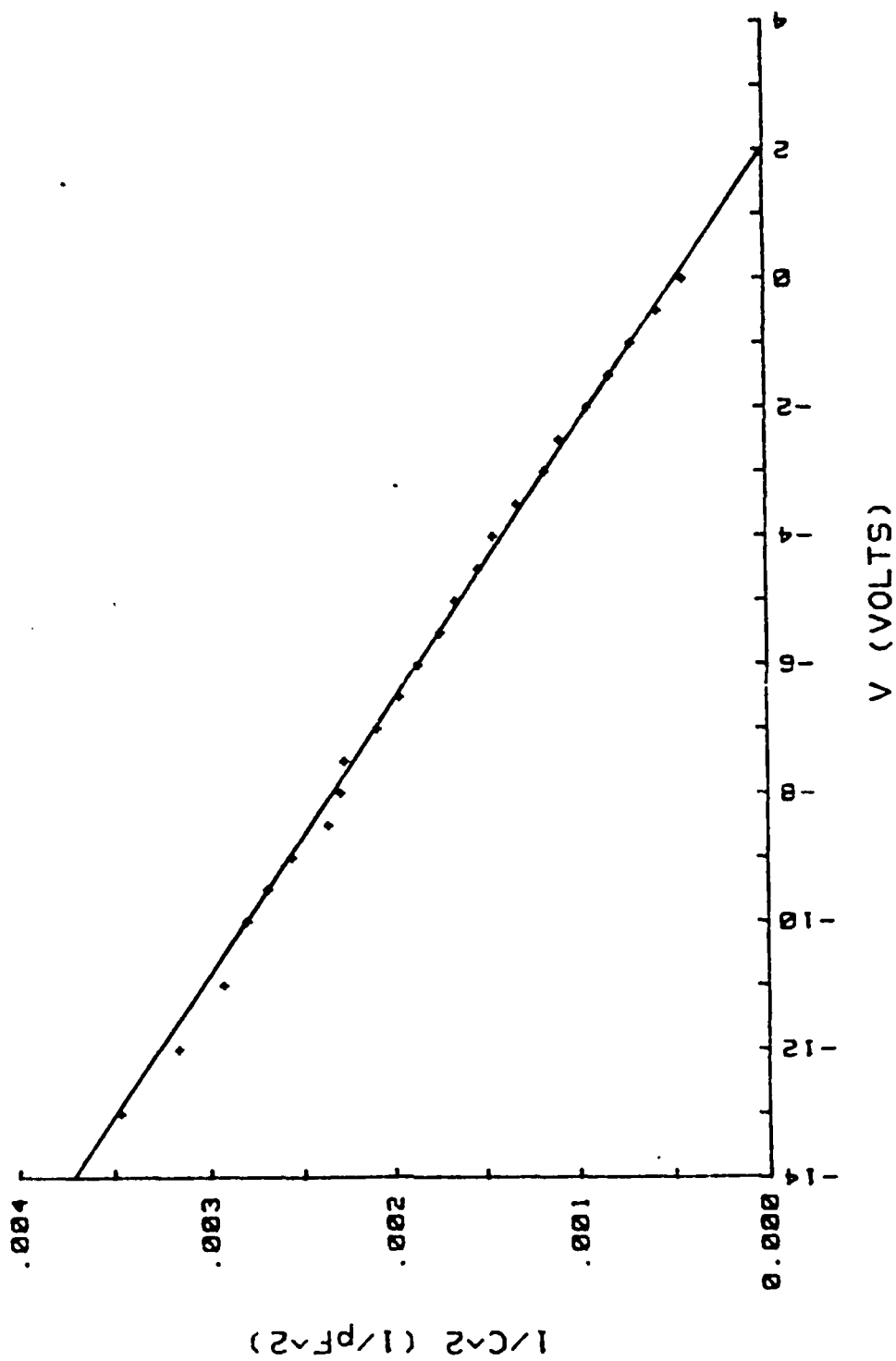
EPITAXIAL InP P/N JUNCTION

InP JFET CONFIGURATION

P (1×10^{18})

S   G   D

N (1×10^{17})

N⁻ $(< 1\times10^{14})$

S.I. InP
(Fe Doped)
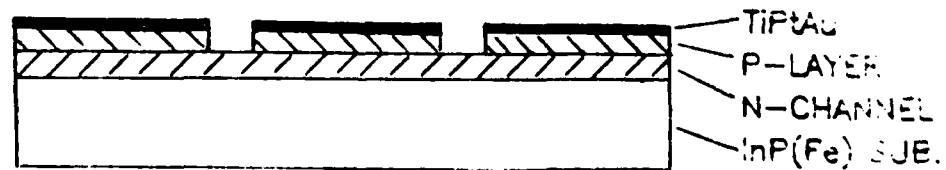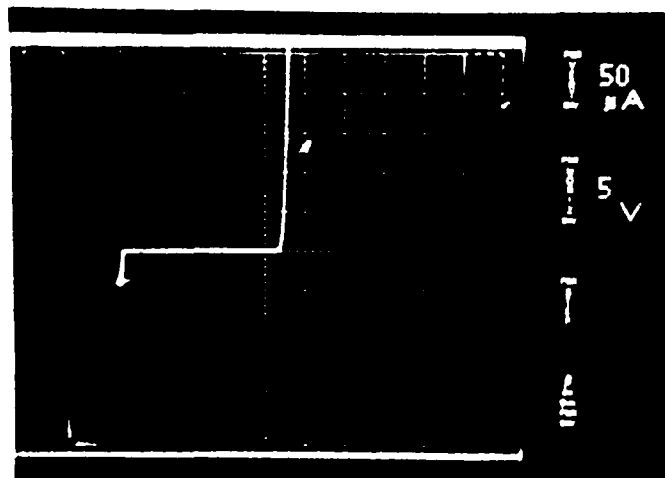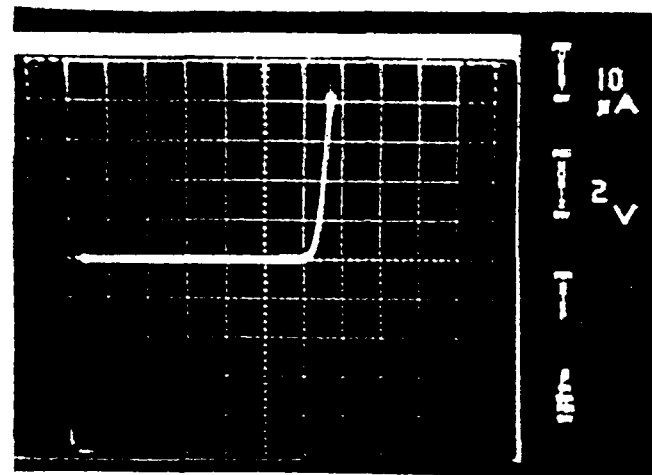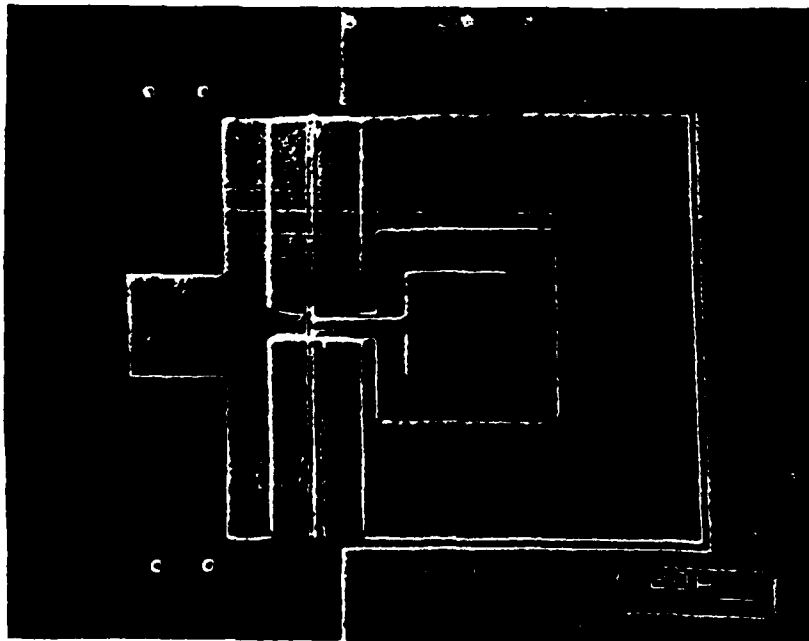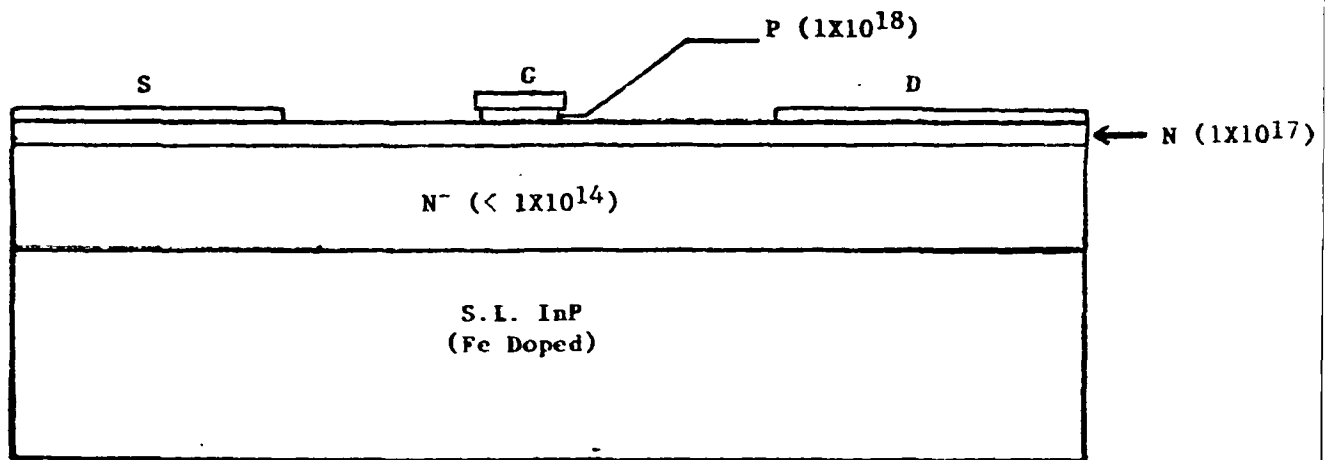
InP FET PROCESS

- MESA ISOLATION

- SOURCE-DRAIN OHMIC CONTACTS

- GATE METAL

- GATE ETCH

- BOND PAD METAL

- PASSIVATION

- BACKSIDE THINNING

- BACKSIDE METAL

- DIE SEPARATION

InP JFET
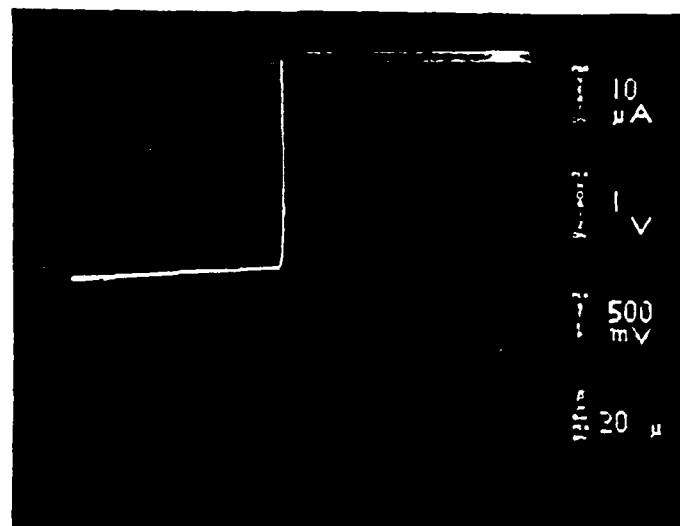
GATE—SOURCE I—V CURVE
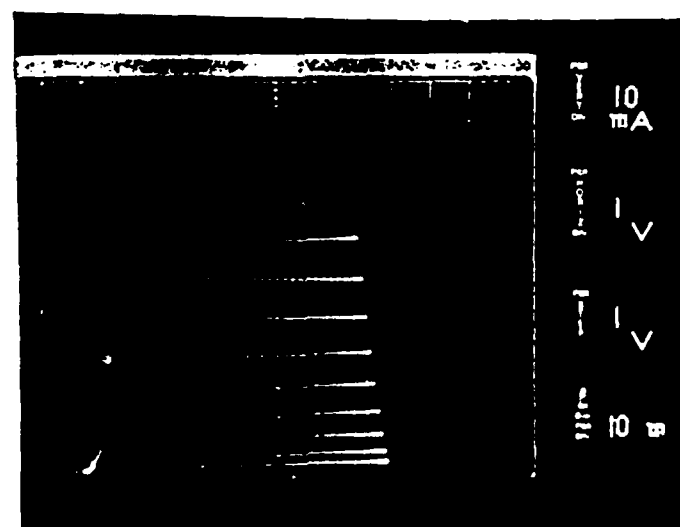
DRAIN—SOURCE I—V CURVES
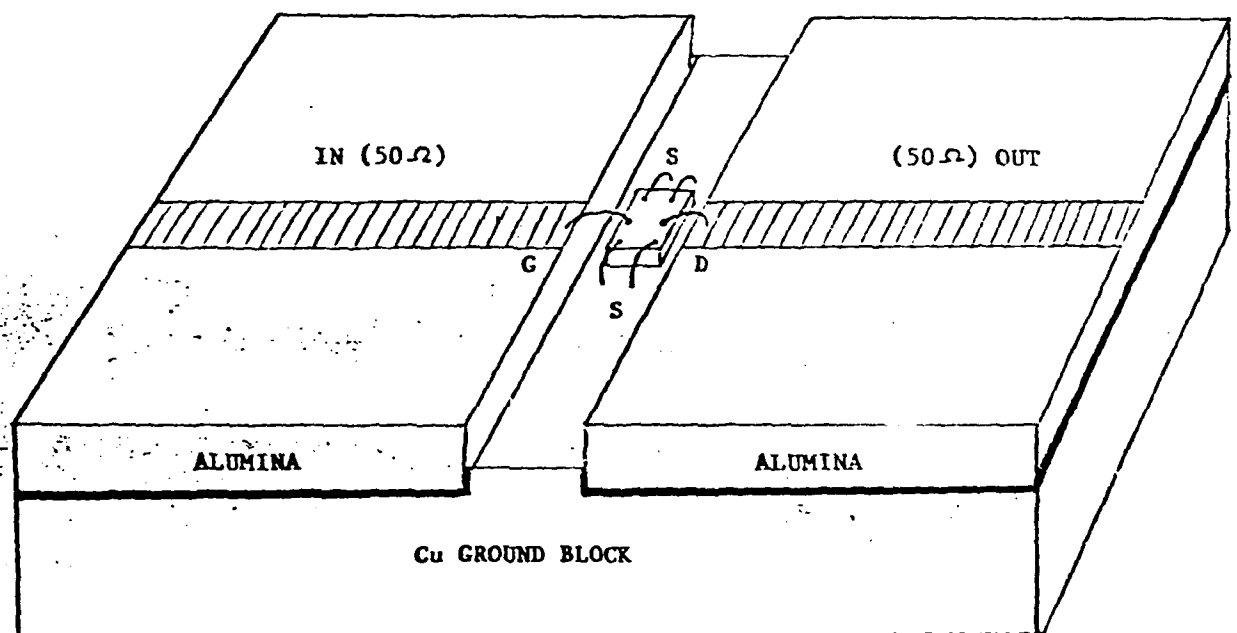
Schematic Representation of Device
Carrier Used for DC and RF Evaluation

InP JFETS

	Lg (um)	Gmo/Z (mS/mm)
BELL LABS	2.0	50
NRL	1.0	40
VARIAN	2.7	50
(VARIAN InP MESFET	1.6	115)

GAIN VS FREQUENCY

JF13
MESFET
Lg=1.6um

JF28
JFET
Lg=2.7um

JF25
JFET
Lg=2.7um

FREQUENCY (GHz)

GAIN(DB)
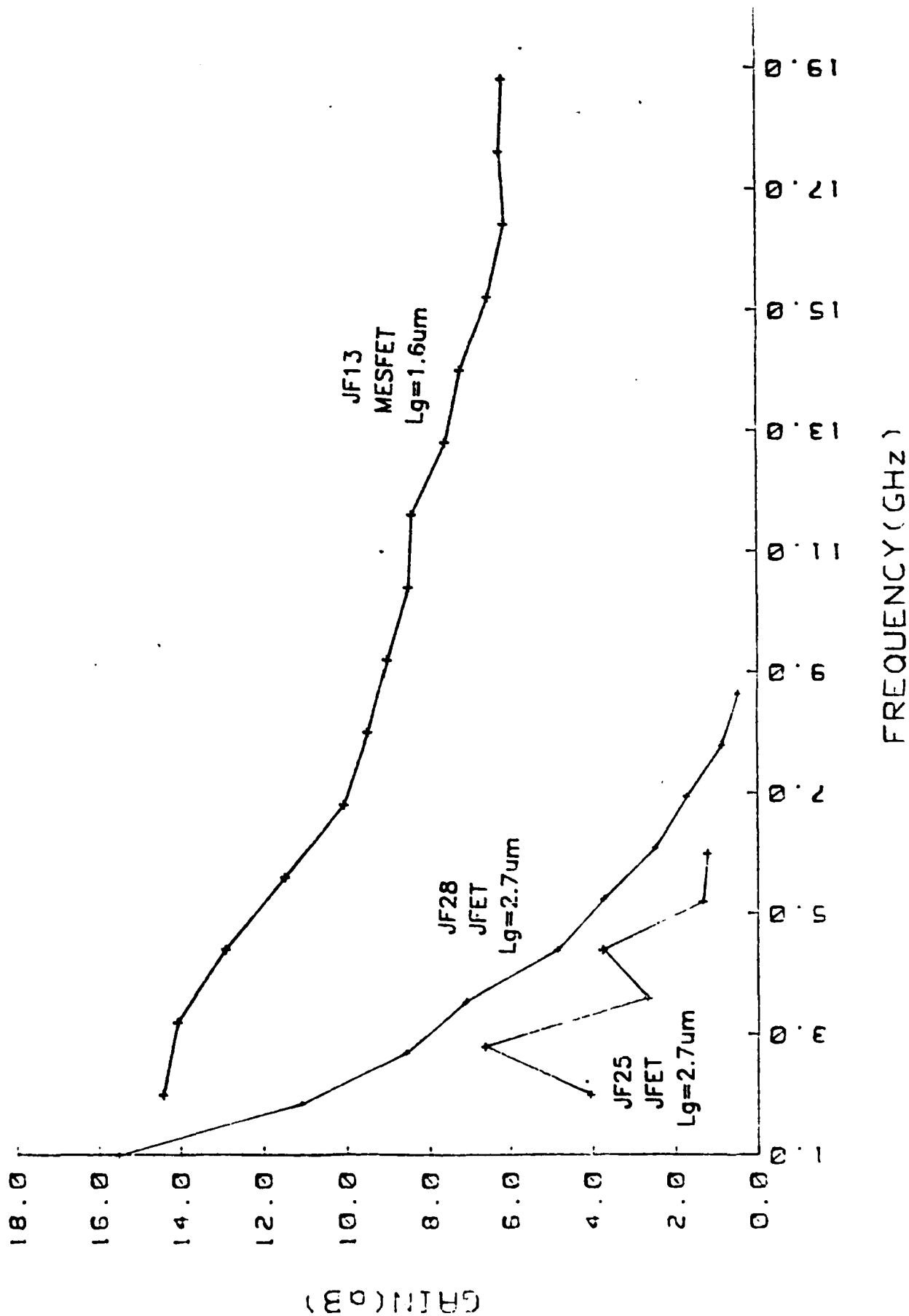
CONCLUSIONS

* GOOD QUALITY InP P/N JUNCTIONS BY VPE

* InP JFETS WITH Gm/Z = 50 mS/mm HAVE BEEN FABRICATED

* CHANNEL CHARACTERISICS APPEAR DEGRADED
    DIFFUSION OF ZINC FROM P-LAYER
    DIFFUSION OF IRON FROM SUBSTRATE

* EXTRINSIC Gm IS LOW DUE TO HIGH Rs

* IMPROVEMENTS NEEDED
    N- BUFFER LAYERS
    LOWER P DOPING TO 1E18 cm^-3
    THIN P-LAYERS
    IMPLANTED N+ SOURCE-DRAIN CONTACTS
    DECREASE GATE LENGTHS TO < 1.0 um

P-DOPING WITH MANGANESE IN MOVPE-GROWN InP AND InGaAs

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P-DOPING WITH MANGANESE IN MOVPE-GROWN InP AND InGaAs

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OUTLINE

1. Summary of MOCVD p-doping issues.

2. Mn doping of InP – dependence on growth parameters.

3. Mn doping of InGaAs – determination of activation energy.

4. p–n junction characteristics.

102

P–DOPANTS FOR III–V MOVPE GROWTH

Typical Dopants: Zn, Cd, Mg, Be

Problems: 1.   Difficult to get reproducibility.

2.   Dopant incorporation is depen–
dent on a variety of growth

parameters:

–   Temperature

–   Chamber Pressure

–   III Concentration

–   V Concentration

–   Dopant Concentration

P-DOPANTS FOR III-V MOVPE GROWTH

Typical Dopants: Zn, Cd, Mg, Be

Problems:

3. Diffusion of dopant species from the p-doped epilayer displaces the p-n junction.

4. Source memory effects during growth prevent sharp turn-on and turn-off of dopant species.

MOVPE GROWTH CONDITIONS:

- ## HORIZONTAL CHAMBER

  1" x 1" CROSS-SECTION

- ## TEMPERATURE, 650°C

- ## PRESSURE, 76 TORR

- ## TMI MOLE FRACTION

  5×10^{-5}

- ## PH_3 MOLE FRACTION

  1×10^{-2}

- ## TOTAL GAS FLOW, 2 SLM

HOLE CARRIER VS DOPANT CONC.

* Mn-InP (300 K)

* Zn-InP (300 K)

Zn (300K)

Zn (77K)

Mn

HOLE CONCENTRATION (CM-3)

Znx10-5 (Mnx10-6)
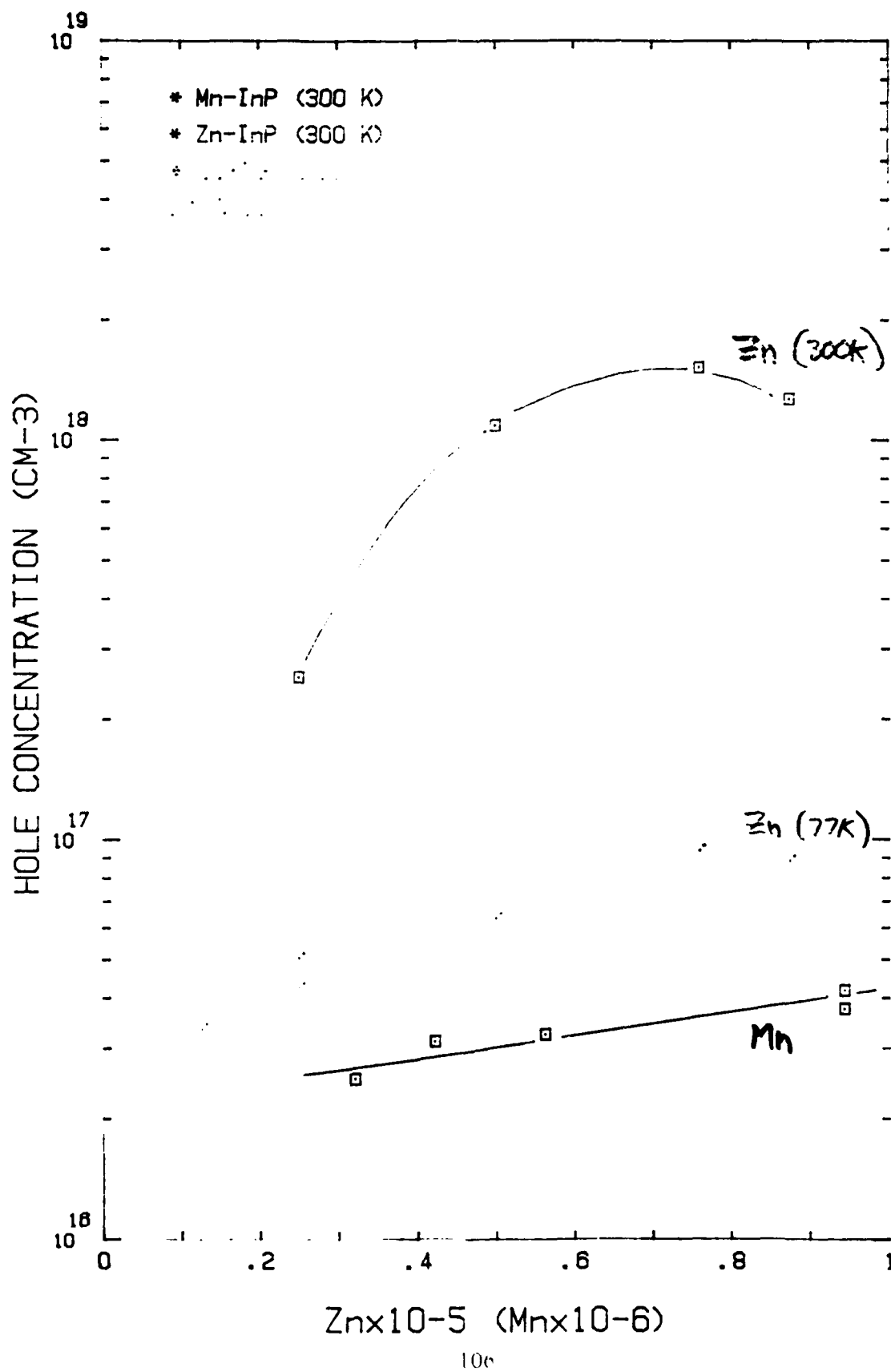
HOLE CARRIER VS TMIn CONC.

Plot of HOLE CONCENTRATION (CM-3) versus TMIn CONCENTRATION (×10-4).

Legend:
* Mn-InP (300 K)
21 sccm TCMn @ RT
* Zn-InP (300 K)
30 sccm DMZn

Zn (300K)

Zn (77K)

Mn
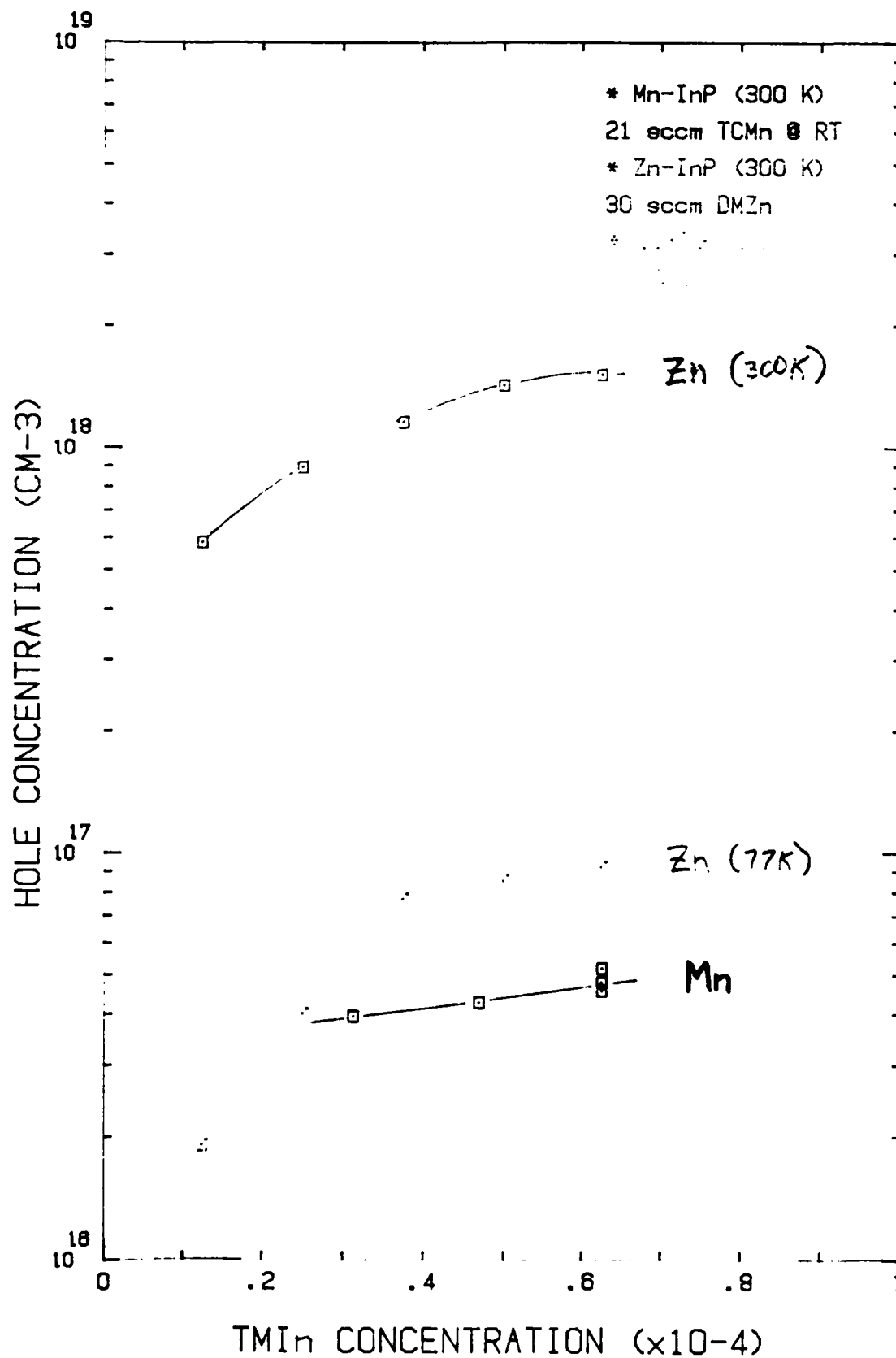
HOLE CARRIER VS PH3 CONC.
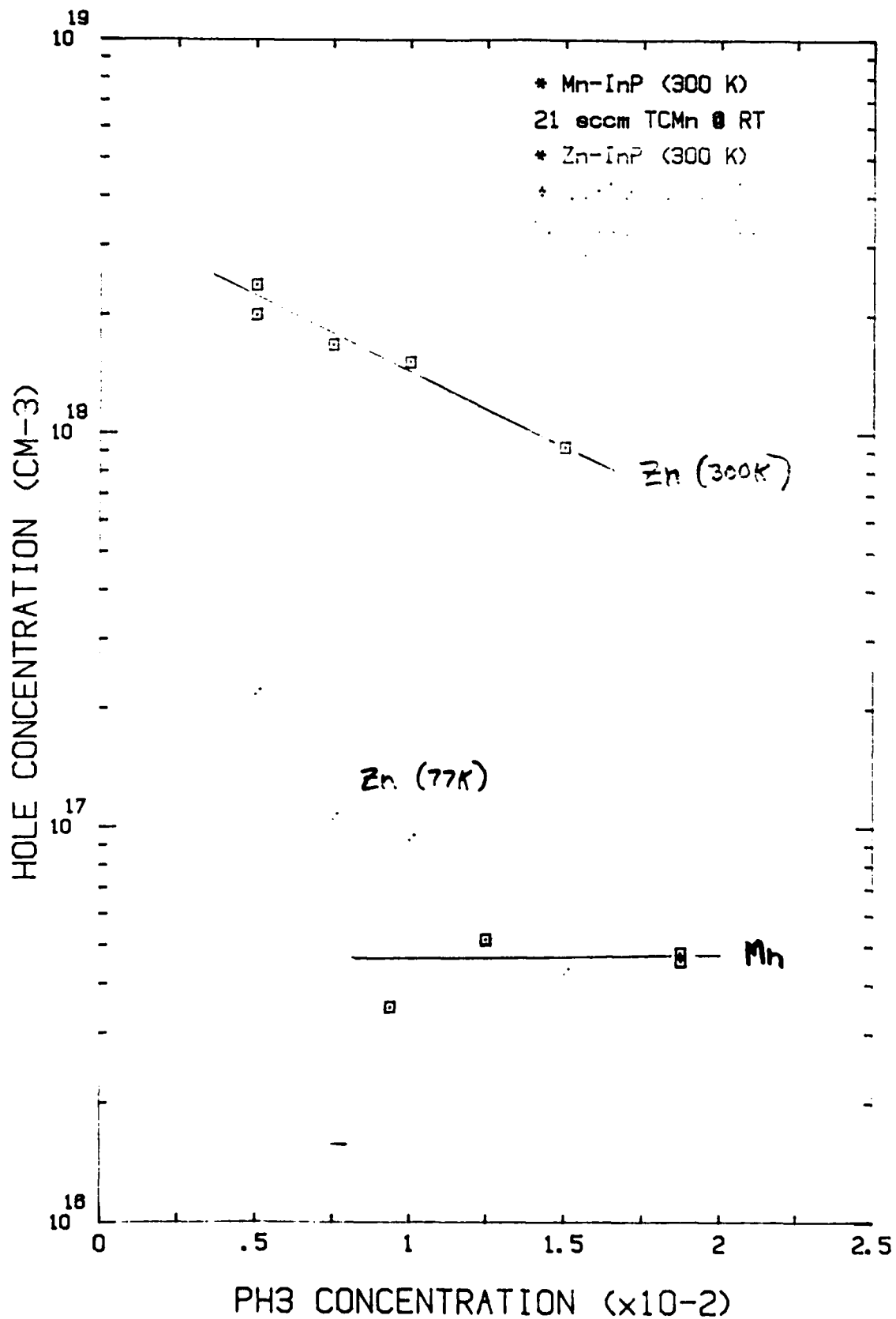
HOLE CARRIER VS PRESSURE

109

Mn-InGaAs

Ea = 52 meV
Na = 2.50E+018 cm-3
Nd = 2.00E+015 cm-3
g = 4
Mv = .6 m

LOG DENSITY (cm-3)

1000/T (K-1)

MU 1449 (MN-DOPED InGaAs/InP:S)   I.VII 7/14/8_
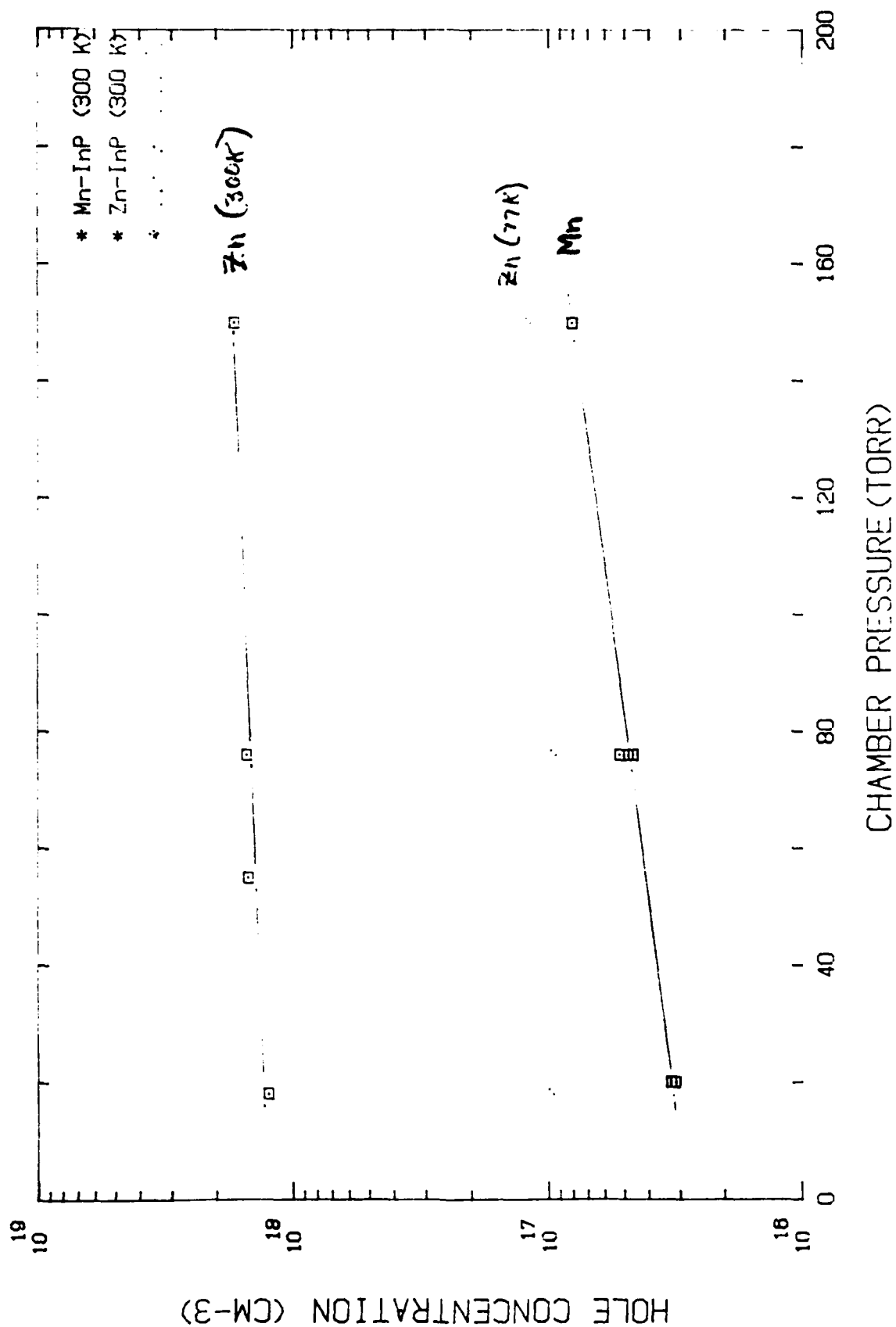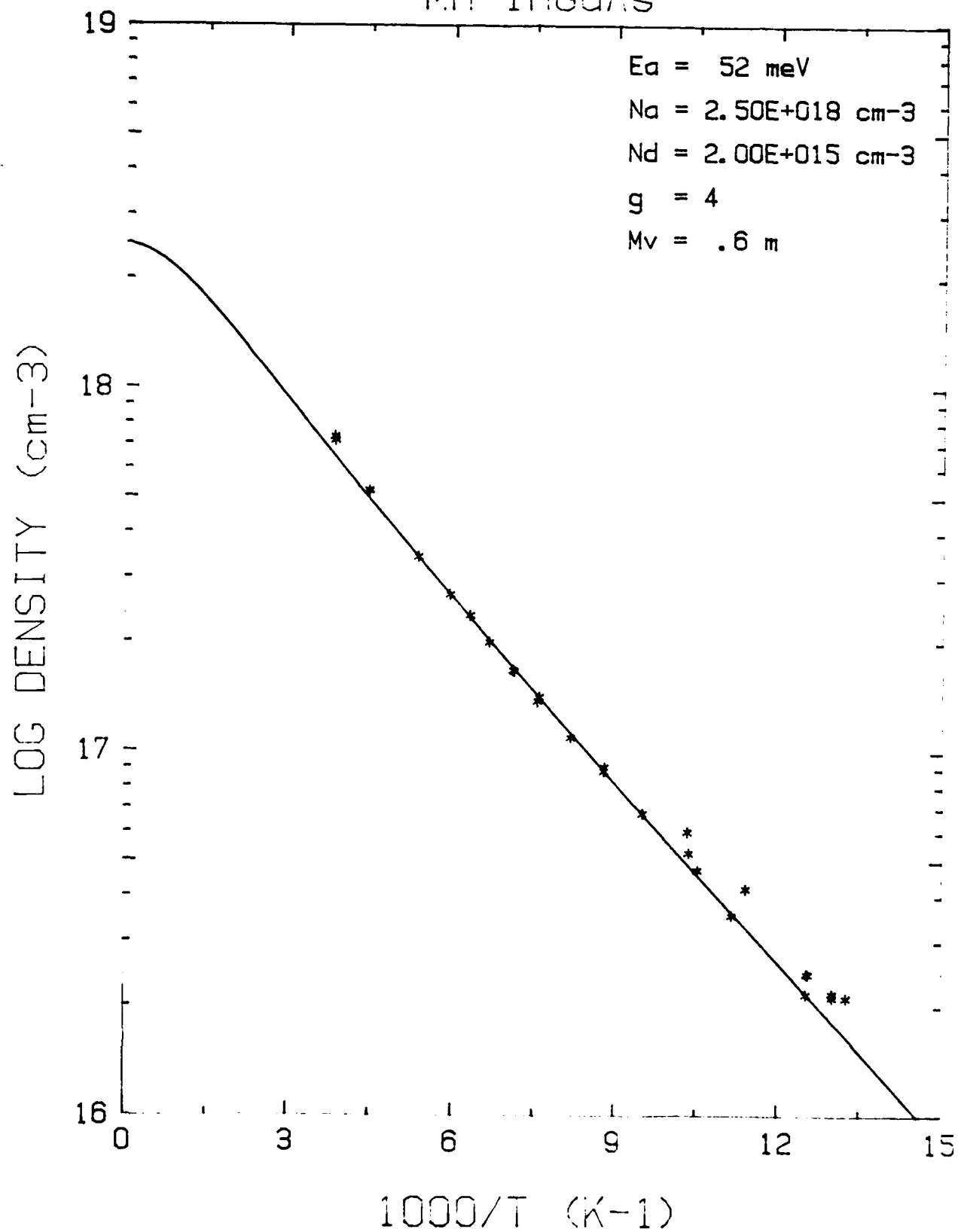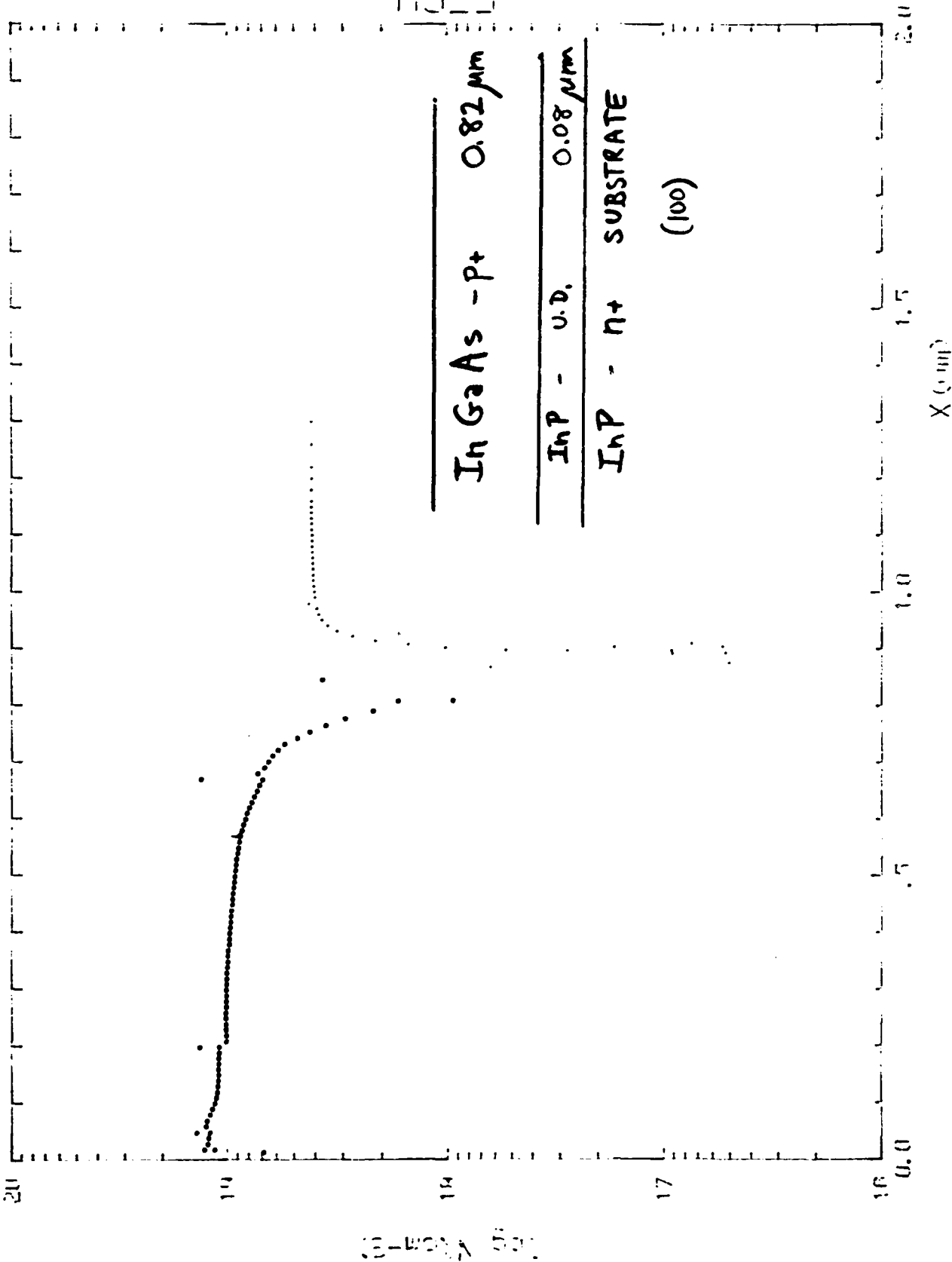
InGaAs - P+   0.82 μm

InP - U.D.   0.08 μm

InP - n+ SUBSTRATE

(100)

ETCH

X (μm)

log N(cm-3)

111

CONCLUSIONS:

1. Controllable p–doping in MOVPE is possible with Mn using tricarbonyl manganese.

2. For InP the deep acceptor level (Ea = 230 mev) limits the usefulness as a dopant to $p < 4 \times 10^{16}$ cm^{-3} .

3. For InGaAs the acceptor level is shown to be Ea = 52 mev; useful for junctions and contacts with $p < 4 \times 10^{18}$ cm^{-3} .

4. There is no evidence of Mn dopant diffusion from the doped epilayer.

InP ON GaAs/Si SUBSTRATES FOR MONOLITHIC INTEGRATION OF ADVANCED HIGH-SPEED OPTOELECTRONICS

Stan Vernon

Spire Corporation
Bedford, MA

InP on GaAs/Si substrates for monolithic integration of advanced high-speed optoelectronics

STAN VERNON
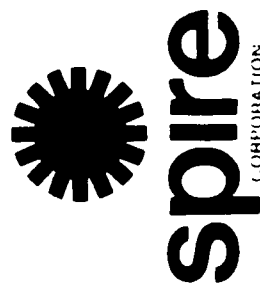
spire
CORPORATION

Bedford, Ma.

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PL – N.M. Haegel (UCLA)

X–RAY – A.T. Macrander (BELL LABS)

   S.J. Pearton

MOCVD – V.E. Haven (SPIRE)

DEVICE – C.J. Keavney (SPIRE)

FUNDING – ARO and NASA Lewis

spire
V–89–07
SMV 1/23/89

116

WHY DEPOSIT InP ONTO GaAs OR Si WAFERS ?

CASE 1. Passive Substrates:

● GaAs or Si wafers compared to InP are:

 - less expensive
 - mechanically stronger
 - higher quality
 - larger areas

CASE 2: Active Substrates:

● For monolithic integration of InP-based components
 (Optoelectronic) with GaAs or Si circuitry (Logic)

✱ spire

V-89-07
SMV 1/23/89

117

DIAGRAM OF POSSIBLE InP-GaAs-Si APPLICATION

I/O for fiber optic communication

High-speed signal processing

Logic circuit and mechanical support

InP

GaInAs

InP

GaAs IC

SI SUBSTRATE OR CIRCUIT
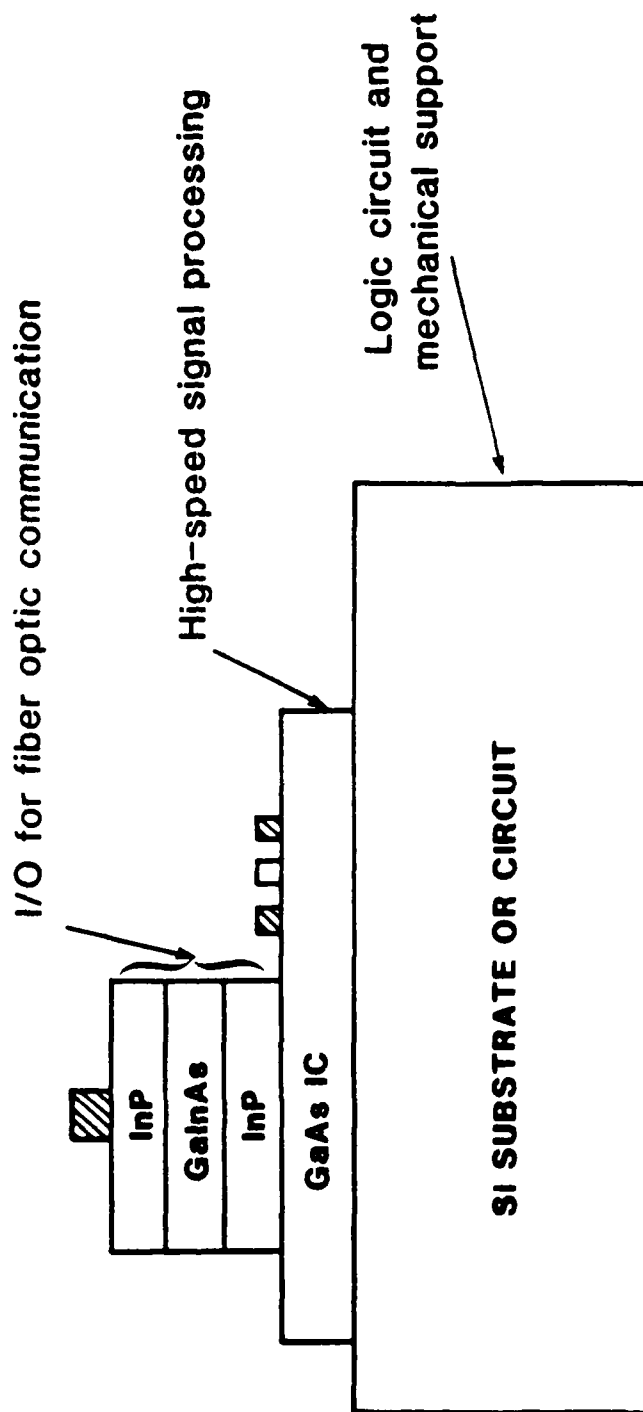
InP-GaAs-Si MATERIAL CONSIDERATIONS

Structure	Lattice Mismatch	Thermal Mismatch	Nucleation
InP/Si	8%	80%	Difficult
GaAs/Si	4%	160%	Moderate
InP/GaAs	4%	-30%	Easy

STRUCTURES STUDIED

1. InP on Si

2. InP on GaAs

3. InP on GaAs on Si

4. InP on InP

GROWTH METHOD

TECHNIQUE: Metalorganic Chemical Vapor Deposition (MOCVD)

REACTOR: SPI-MO CVD 450

- five 2" wafers

- vertical, rotating, barrel geometry

GROWTH PARAMETERS

InP

- 1 atm. pressure
- TmIn + PH_3
- 4 μm/hr
- 600°C

GaAs on Si

- 1 atm. pressure
- TmGa + AsH_3
- 4 μm/hr
- 3-step growth
  - 1050°C bakeout
  - 400°C nucleation
  - 675°C deposition

EXPERIMENTAL RESULTS

- Optical microscopy

- X-ray analysis

- Transmission electron mocroscopy

- Low-temperature photoluminescence

- Electrical measurements

- Device data

SURFACES OF InP DIRECTLY ON Si
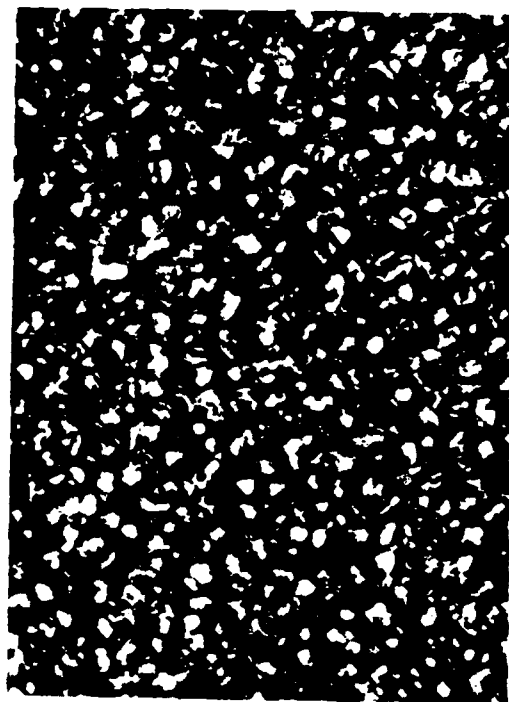
(111)
SILICON
1000X

25 MICRONS

(100)
SILICON
1000X

SURFACES OF TWO-STEP InP ON Si
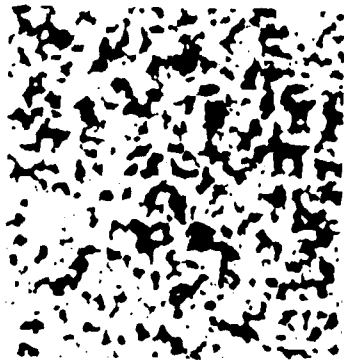
7 SEC
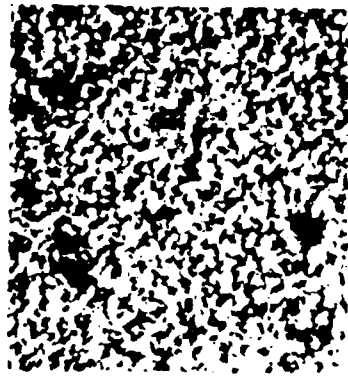
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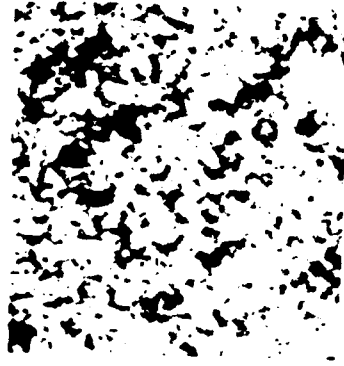
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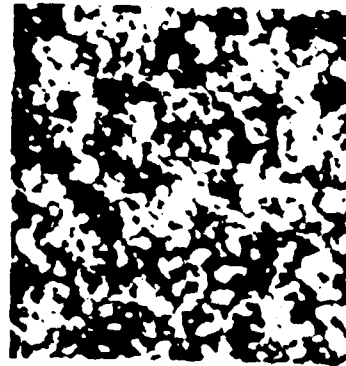
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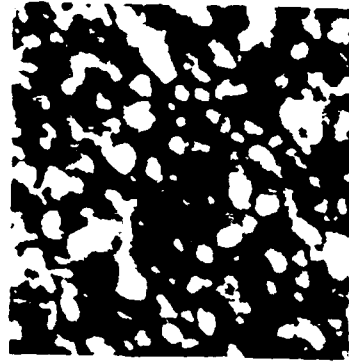
120 SEC

200 SEC

25 MICRONS

124

SURFACES OF InP ON Si WITH In PRELAYER

1000X

5 SEC In LAYER

1000X

10 SEC In LAYER

1000X

20 SEC In LAYER

25 MICRONS

SURFACES OF 1 μm InP–GaAs–Si

200Å GaAs
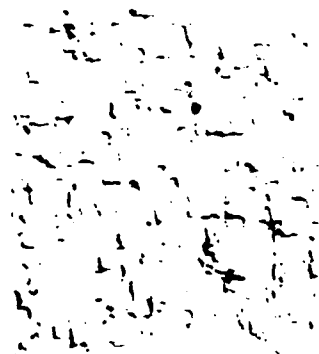
400Å GaAs

1000Å GaAs

~4μm GaAs

1μm GaAs

SURFACES OF InP-GaAs-Si AND GaAs-Si

1000X

3μm GaAs/Si

25 MICRONS

1000X

2μm InP/Si WITH 1μm
GaAs INTERMEDIATE LAYER

127

X-RAY DIFFRACTOMETER SCANS OF InP ON Si
WITH AND WITHOUT A THIN GaAs BUFFER LAYER

128
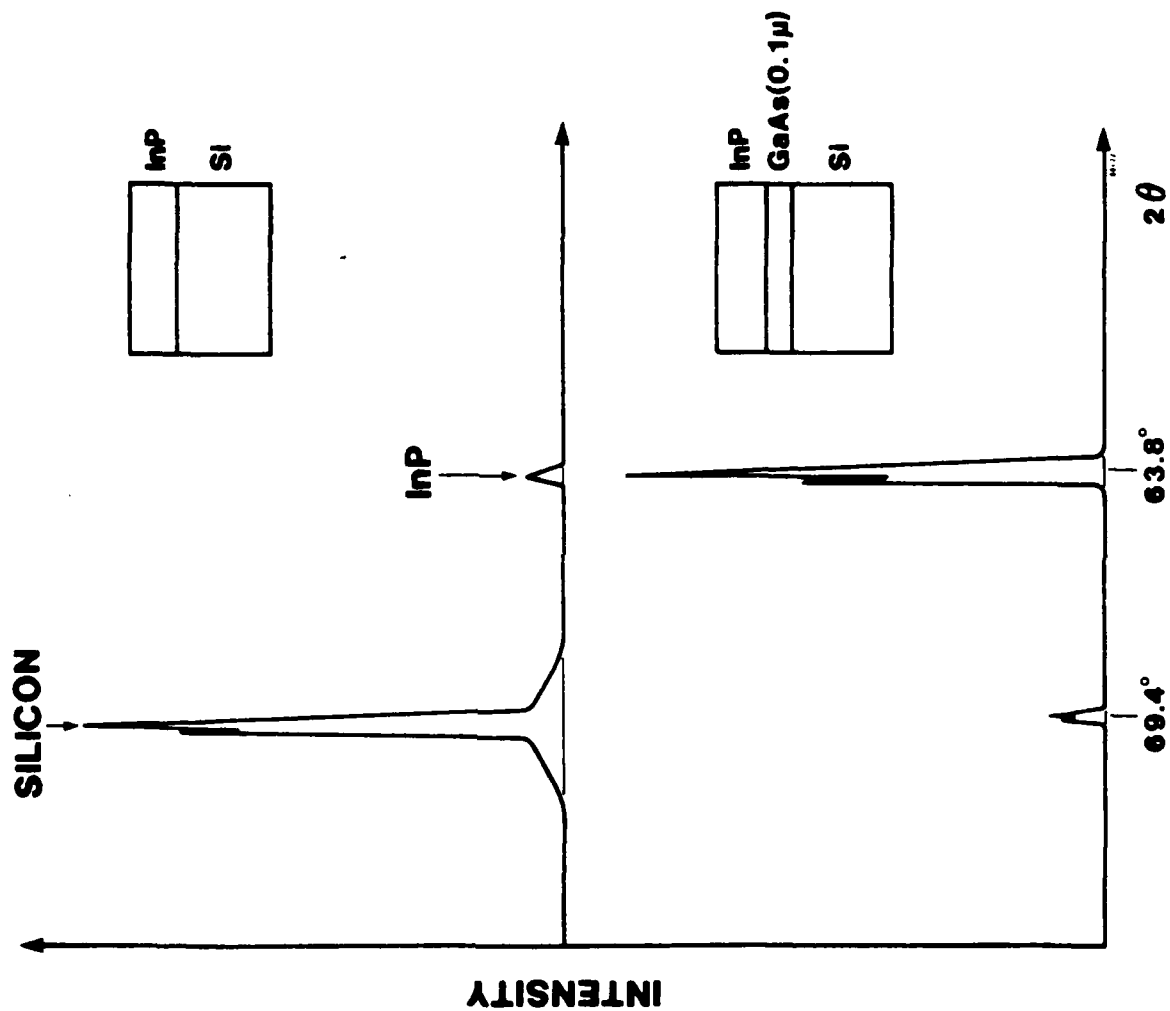
XRRC DATA FOR InP ON Si WITH AND WITHOUT GaAs BUFFER
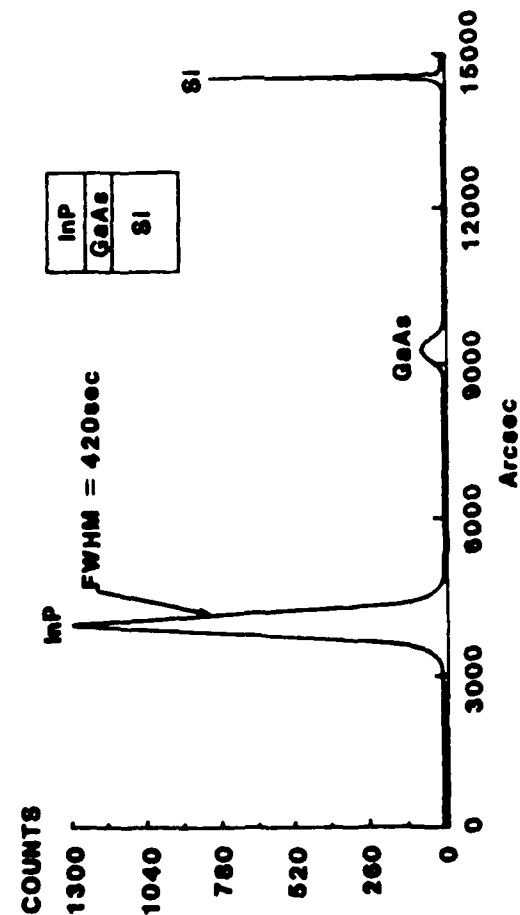
a. InP ON GaAs ON Si
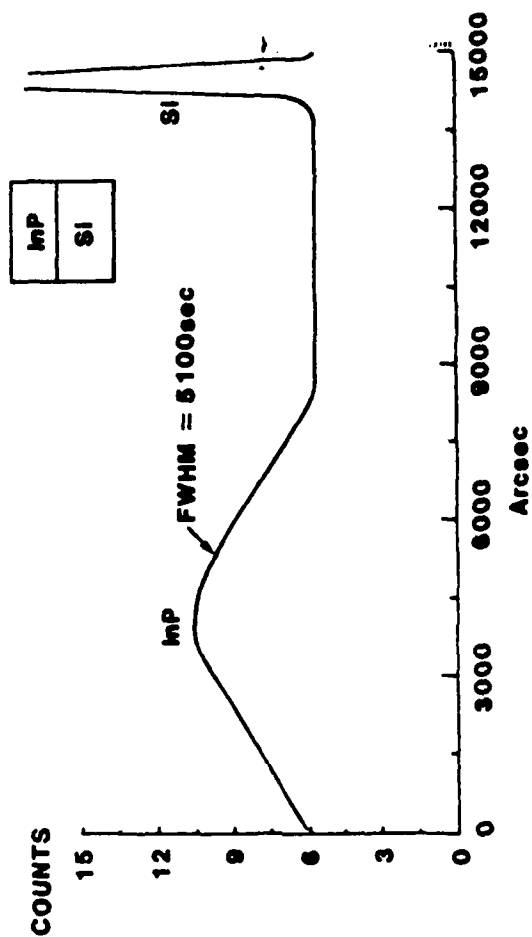
b. InP ON Si

129

InP-GaAs-Si X-RAY ROCKING CURVE RESULTS
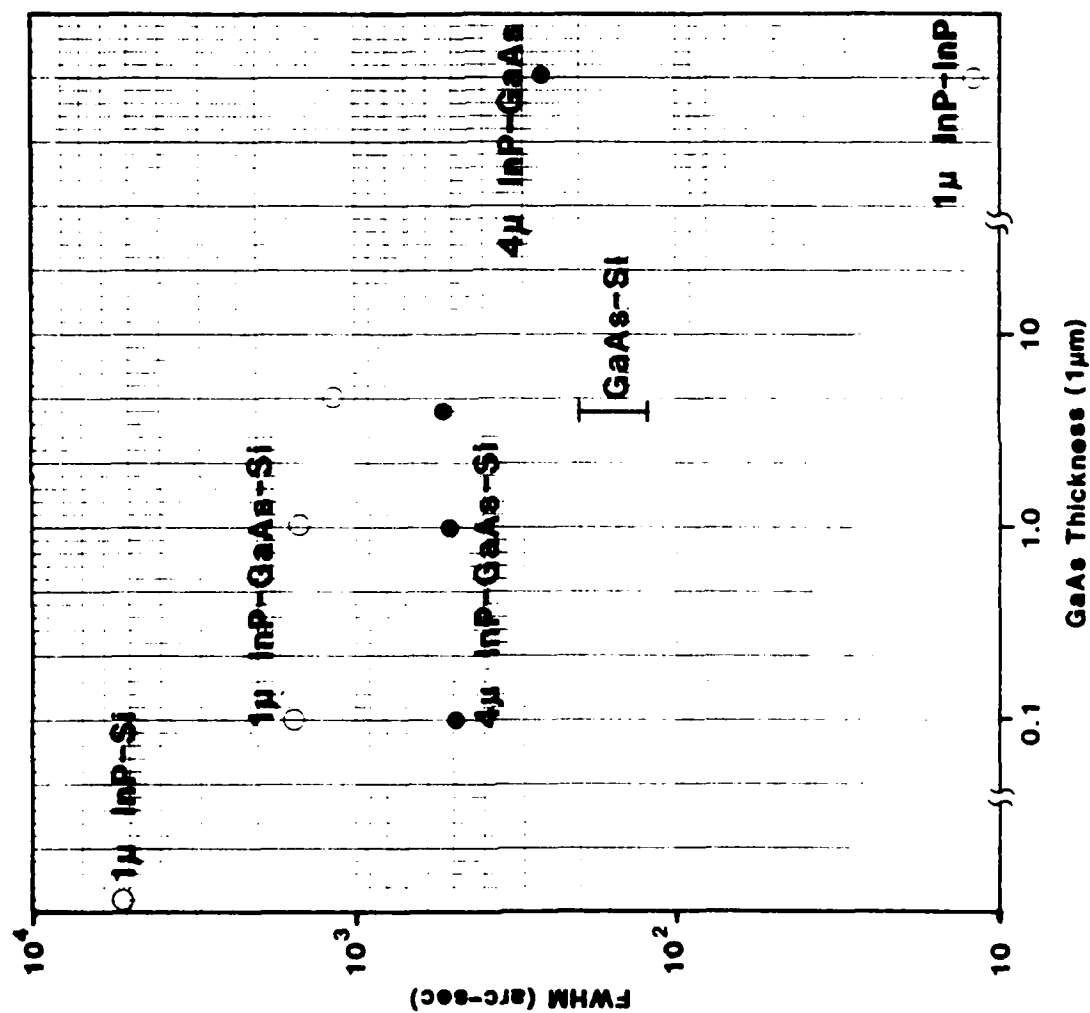
PLANVIEW TEM OF InP-GaAs-Si

STACKING FAULT

DISLOCATION

1μm
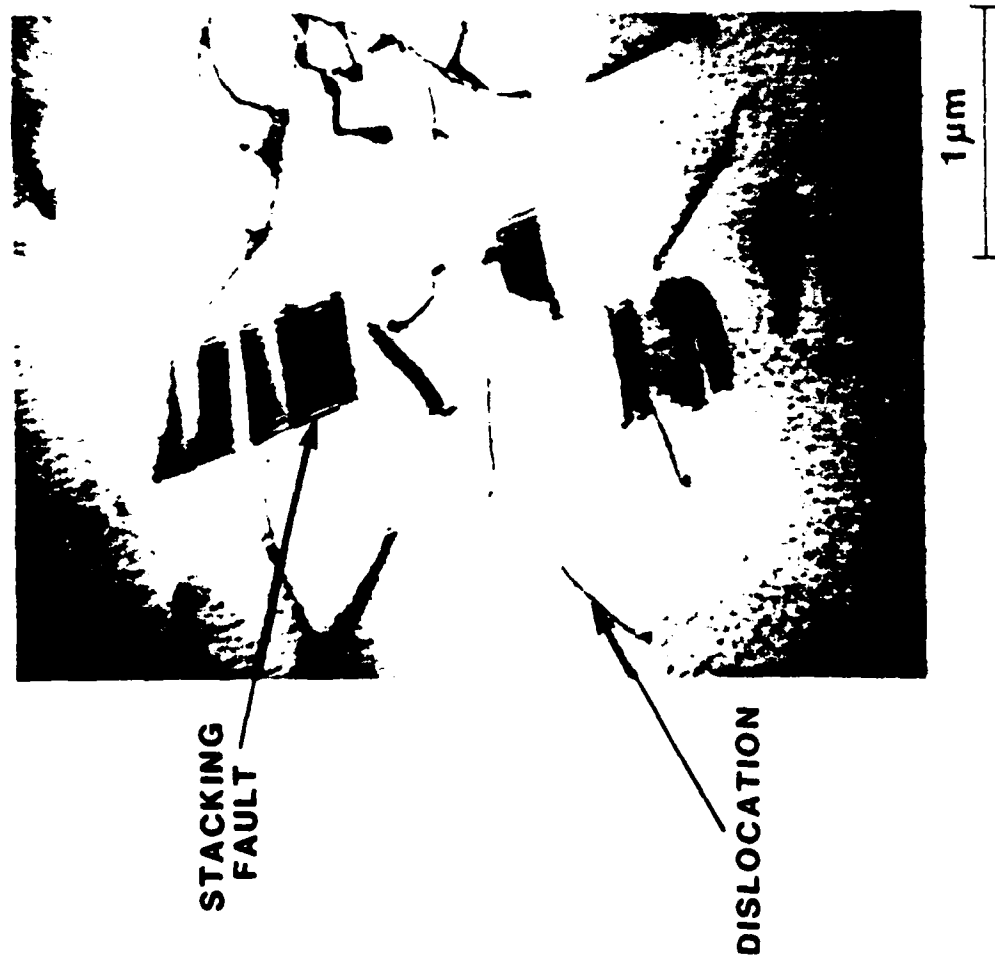
InP THICKNESS = 4μm, GaAs THICKNESS = 1μm

CROSS-SECTION TEM OF InP-GaAs-Si

InP

GaAs

Si

InP THICKNESS = 4μm. GaAs THICKNESS = 1μm

132
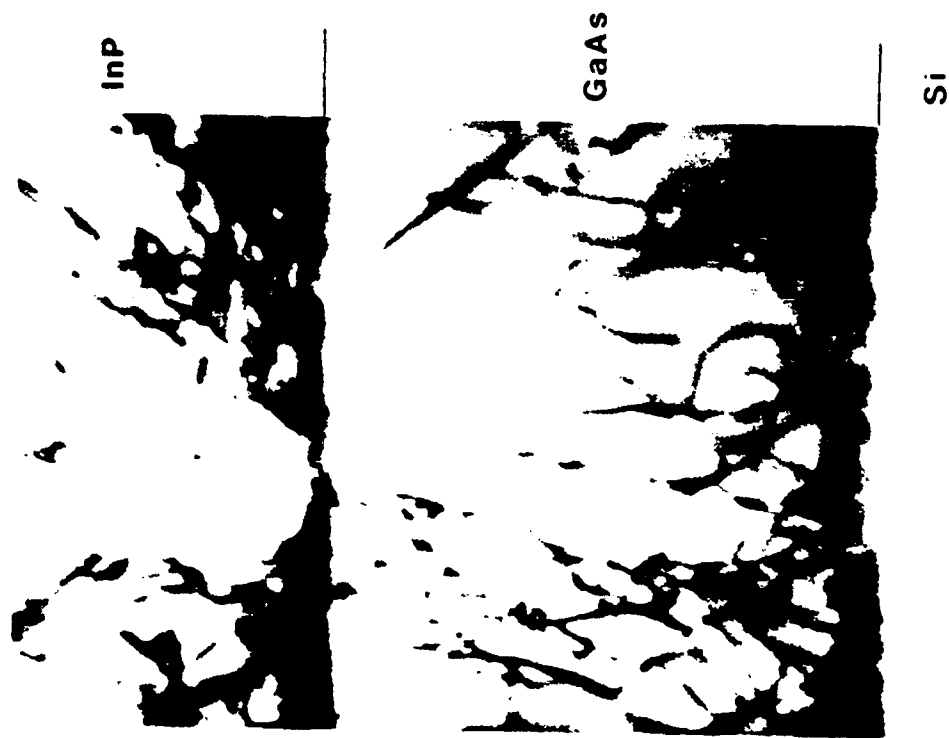
TYPICAL DOPING PROFILE OF InP-GaAs-Si

133
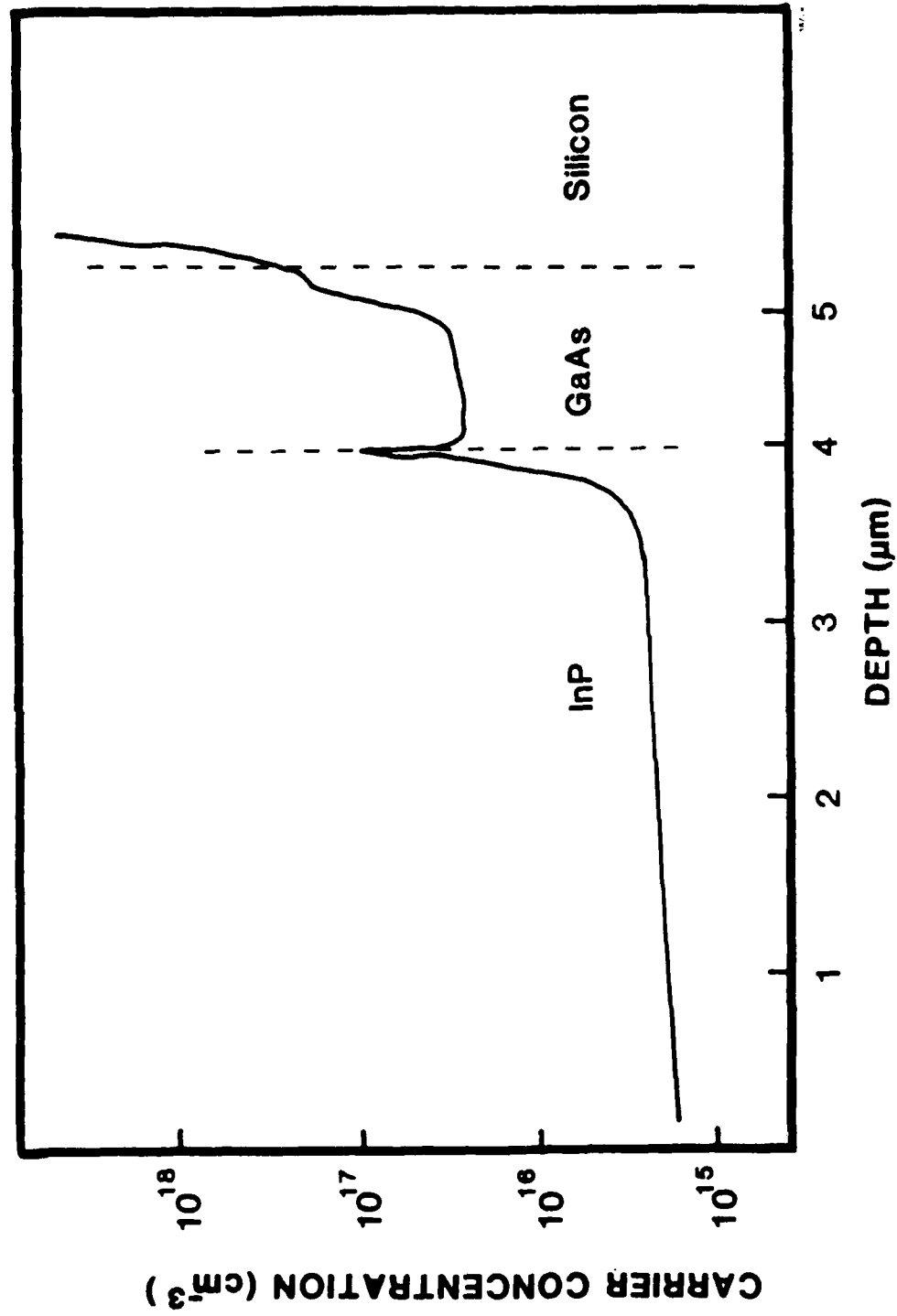
HALL EFFECT DATA FOR InP LAYERS ON S.I. SUBSTRATES

InP layers are 4 um, undoped

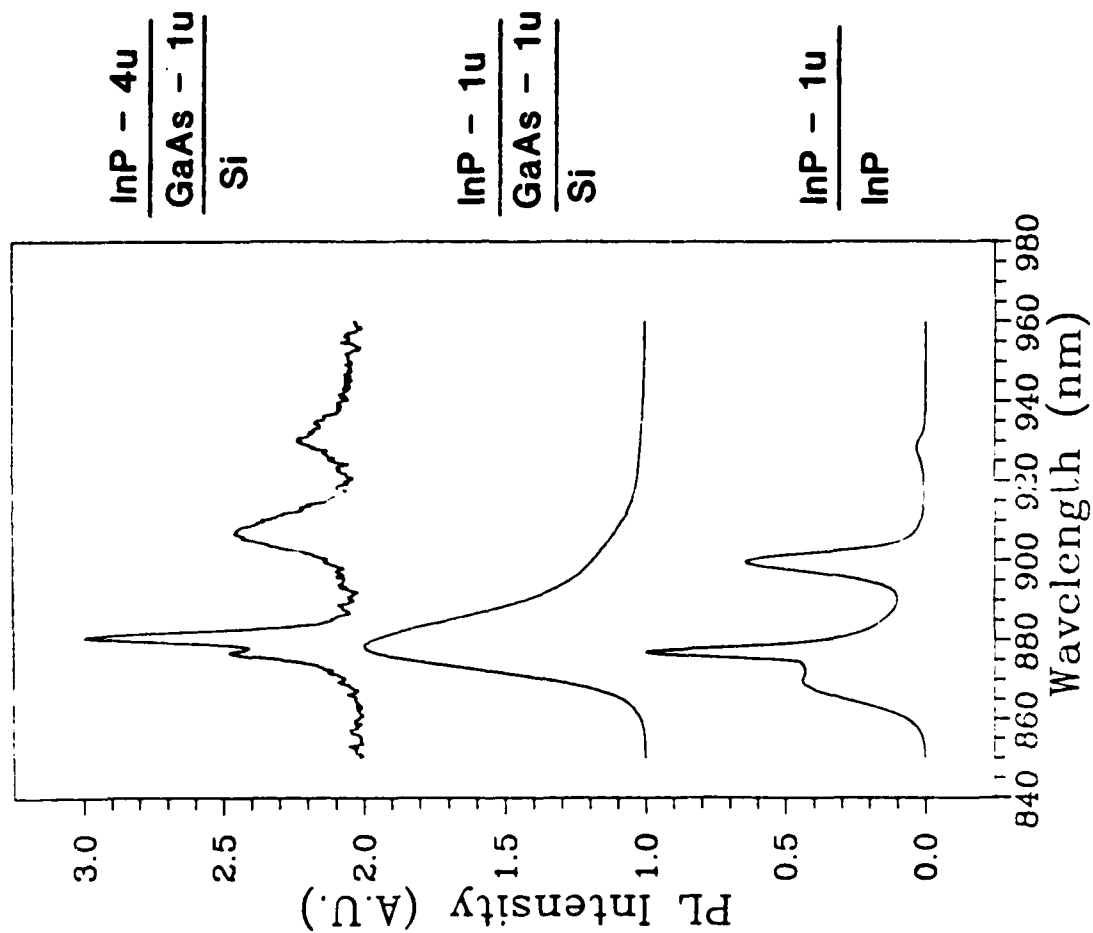| Substrate	AT 77°K		AT 300°K	
	N(cm³)	µ(cm²/v–sec)	N(cm³)	µ(cm²/v–sec)
GaAs	4E14	12,000	9E14	1800
InP	6E14	34,000	9E14	3100

134
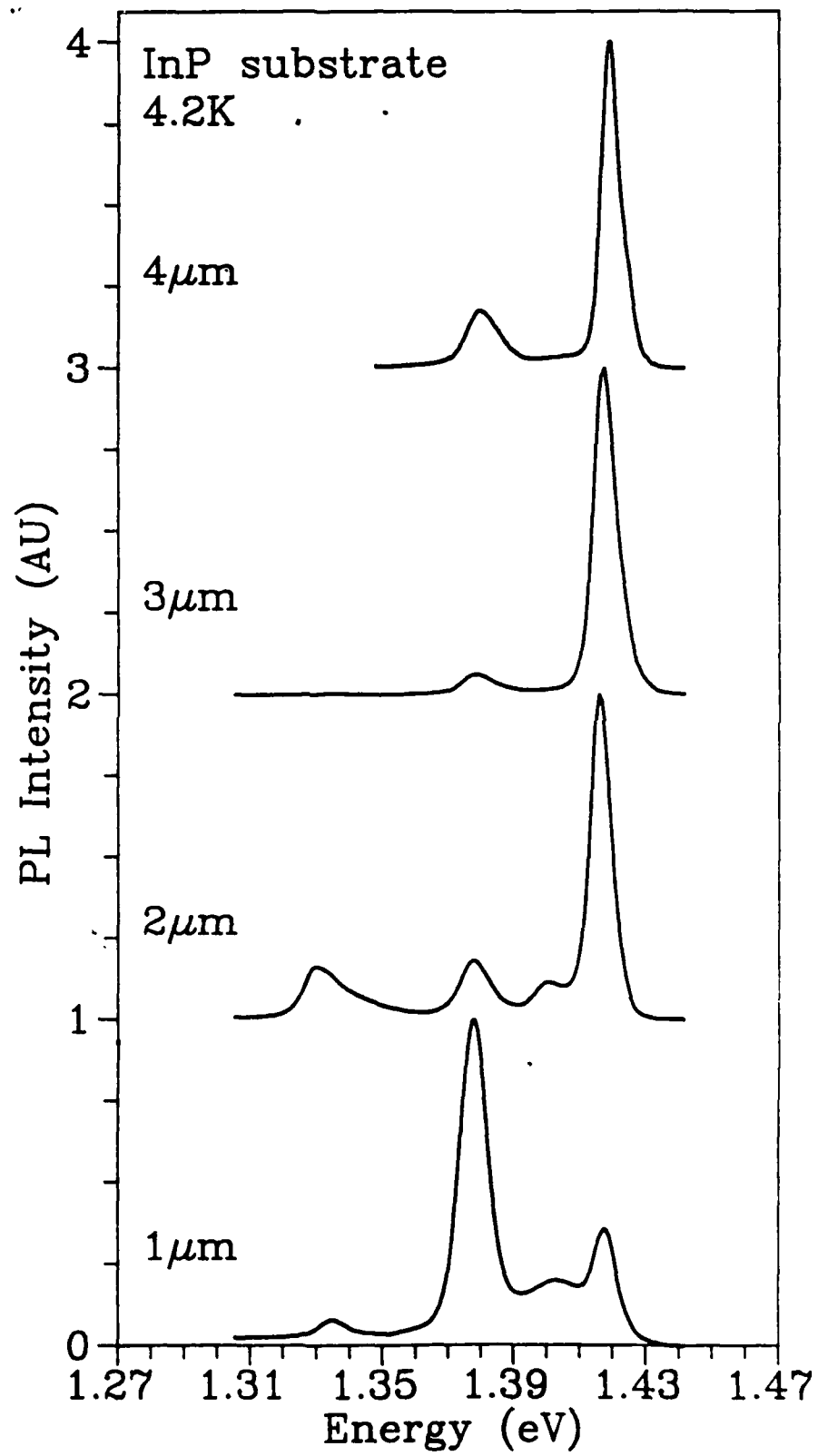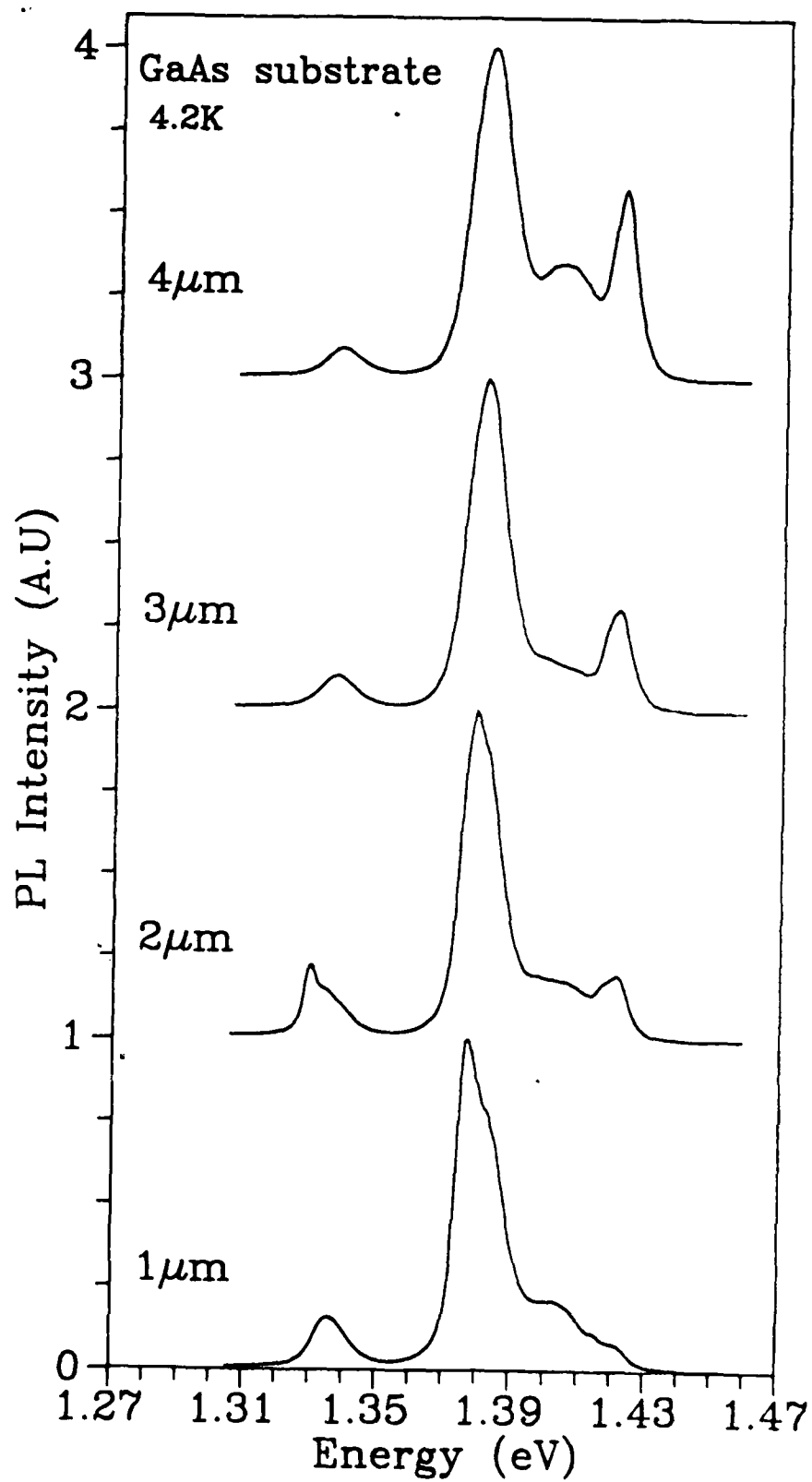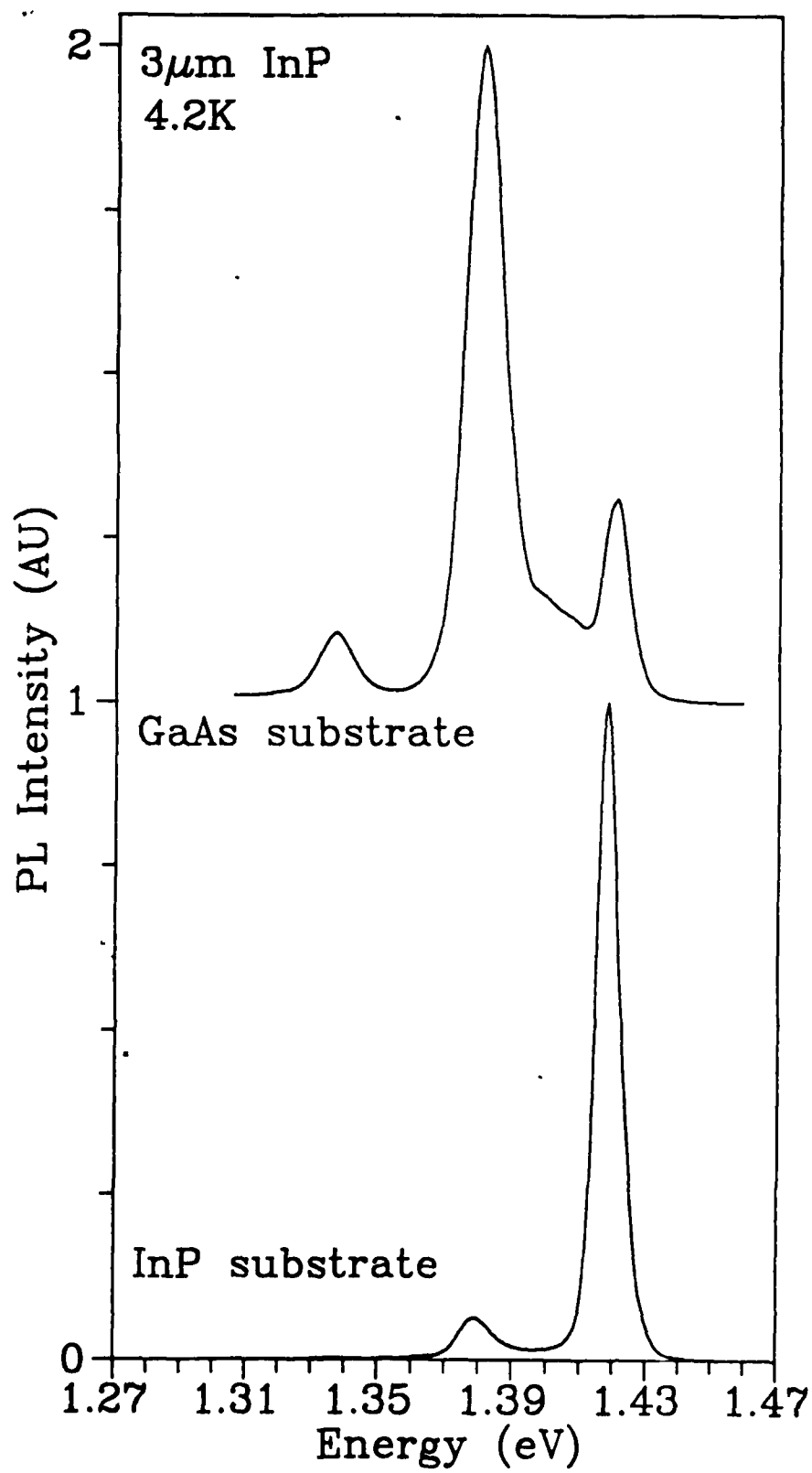
4.4°K PHOTOLUMINESCENCE DATA

138

DIAGRAM OF SOLAR CELL DEVICE STRUCTURES

Front Grid — Cr/Au/Ag

DLARC — ZnS/MgF

Emitter — N⁺ InP (.05μ)

Base — P InP (3μ)

Buffer — P⁺ InP (1μ)

Substrate — P⁺ InP, GaAs, GaAs (1μ) / Si

Back Contact — Au-Zn, Au-Zn, Al-Ti-Pd-Ag

Light

spire
V-89-07
SMV 1/23/89

139
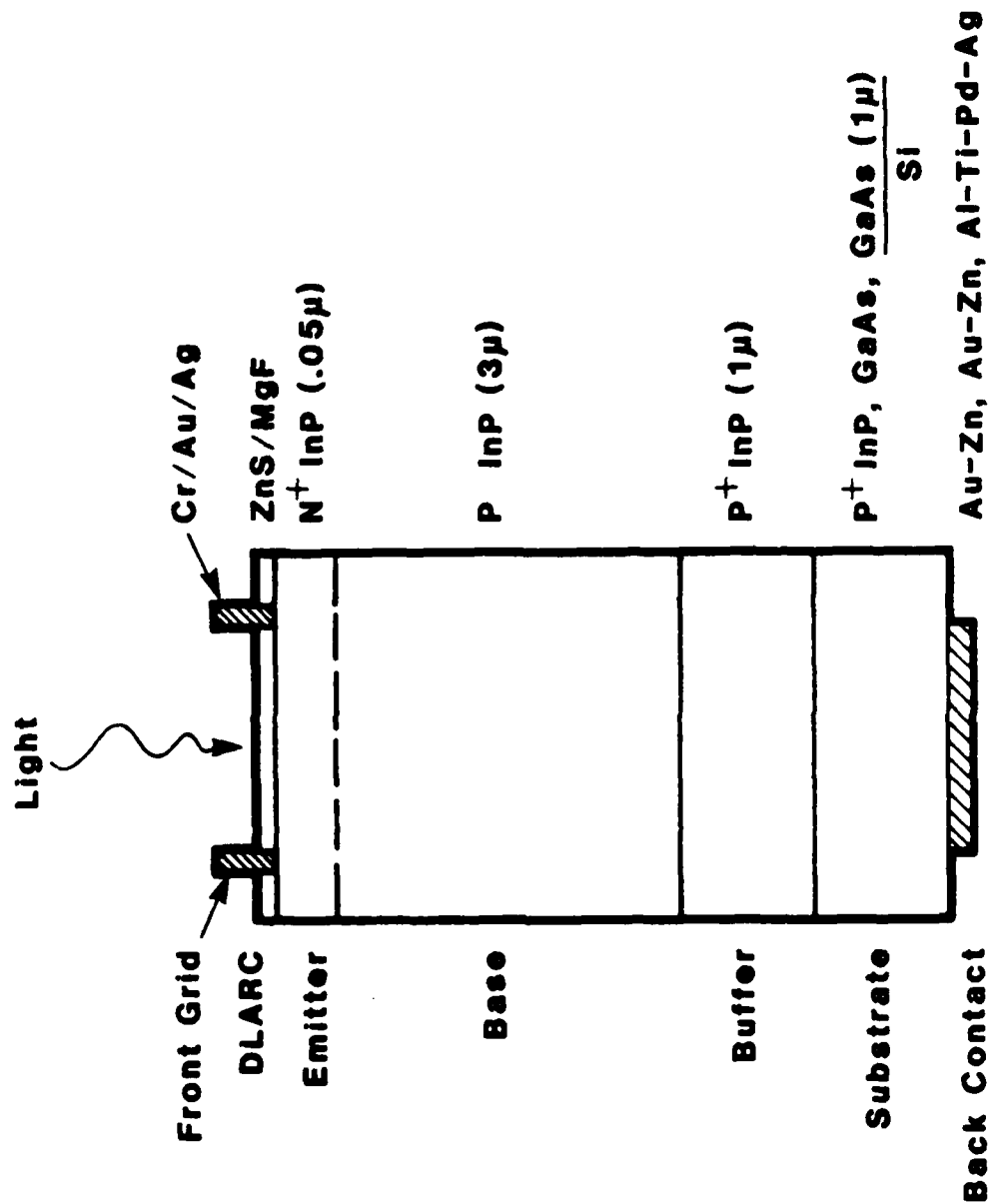
SOLAR CELL DEVICE RESULTS

Structure	Efficiency (%)	Comments
InP–GaAs–Si	7.2	contact to InP
InP–GaAs	9.4	
InP–InP	9.9	surface pitted
InP–InP	17.9	previous best

DEVICE SIZE: 0.5X0.5 cm

TEST CONDITIONS: 1 sun, AMO, 25°C

SPECTRAL RESPONSE OF InP CELLS
ON VARIOUS SUBSTRATES

— silicon substrate
— — GaAs substrate
· · · InP substrate
—·— calculated for L = 0.25 μm

wavelength (nm)

internal quantum efficiency
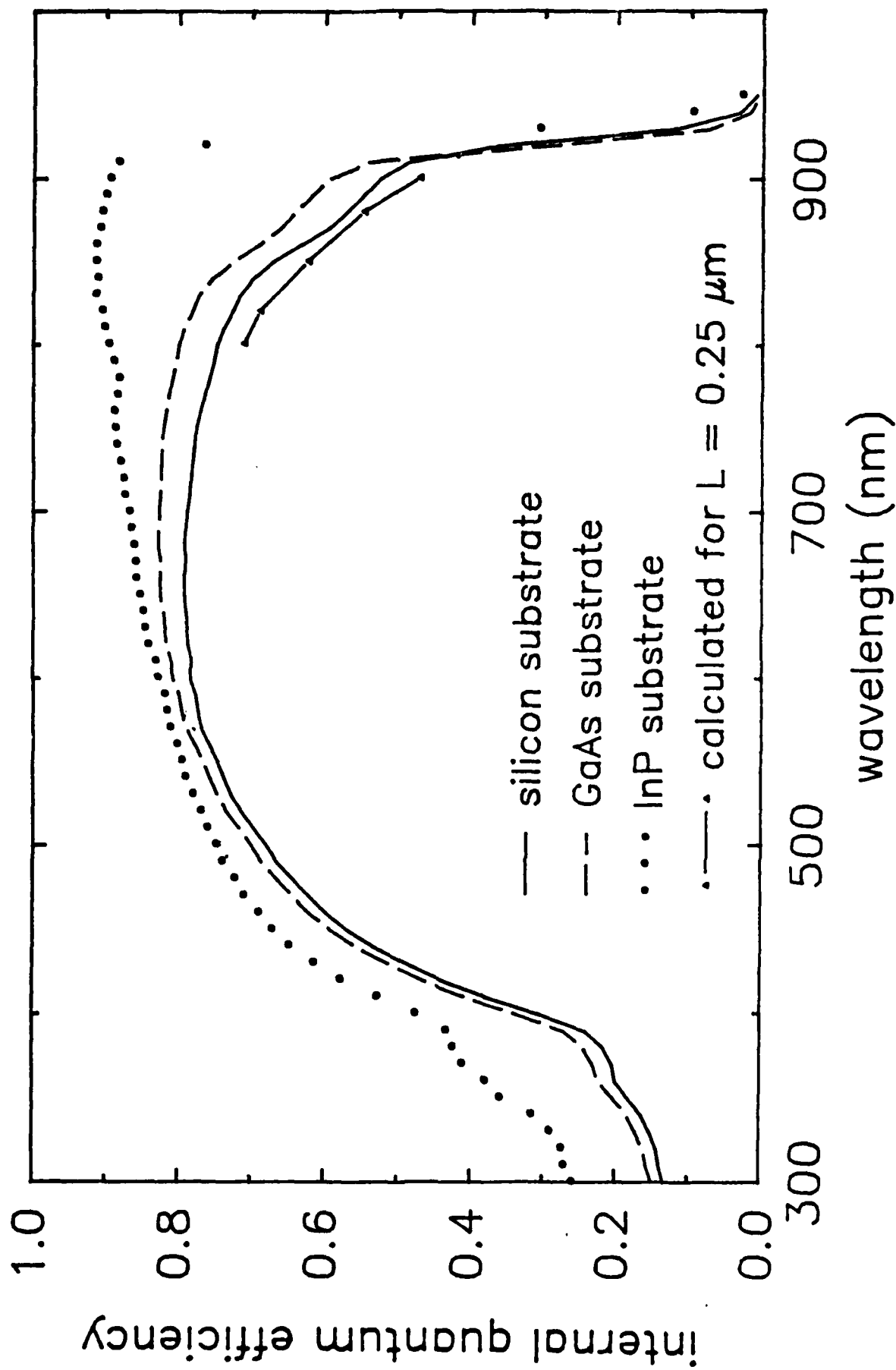
SUMMARY

- InP–GaAs–Si structures may be useful for monolithic integration of optoelectronic and IC functions

- GaAs buffer layers facilitate InP/Si growth and utilize the large GaAs/Si technology base

- Single-crystal InP/GaAs/Si and InP/GaAs structures have been grown by a large-area MOCVD process

- These structures have been characterized and shown to possess fairly good material properties

- Fabrication and testing of preliminary minority-carrier devices show promising results

- Defect-reduction studies have just begun and significant material improvements are expected

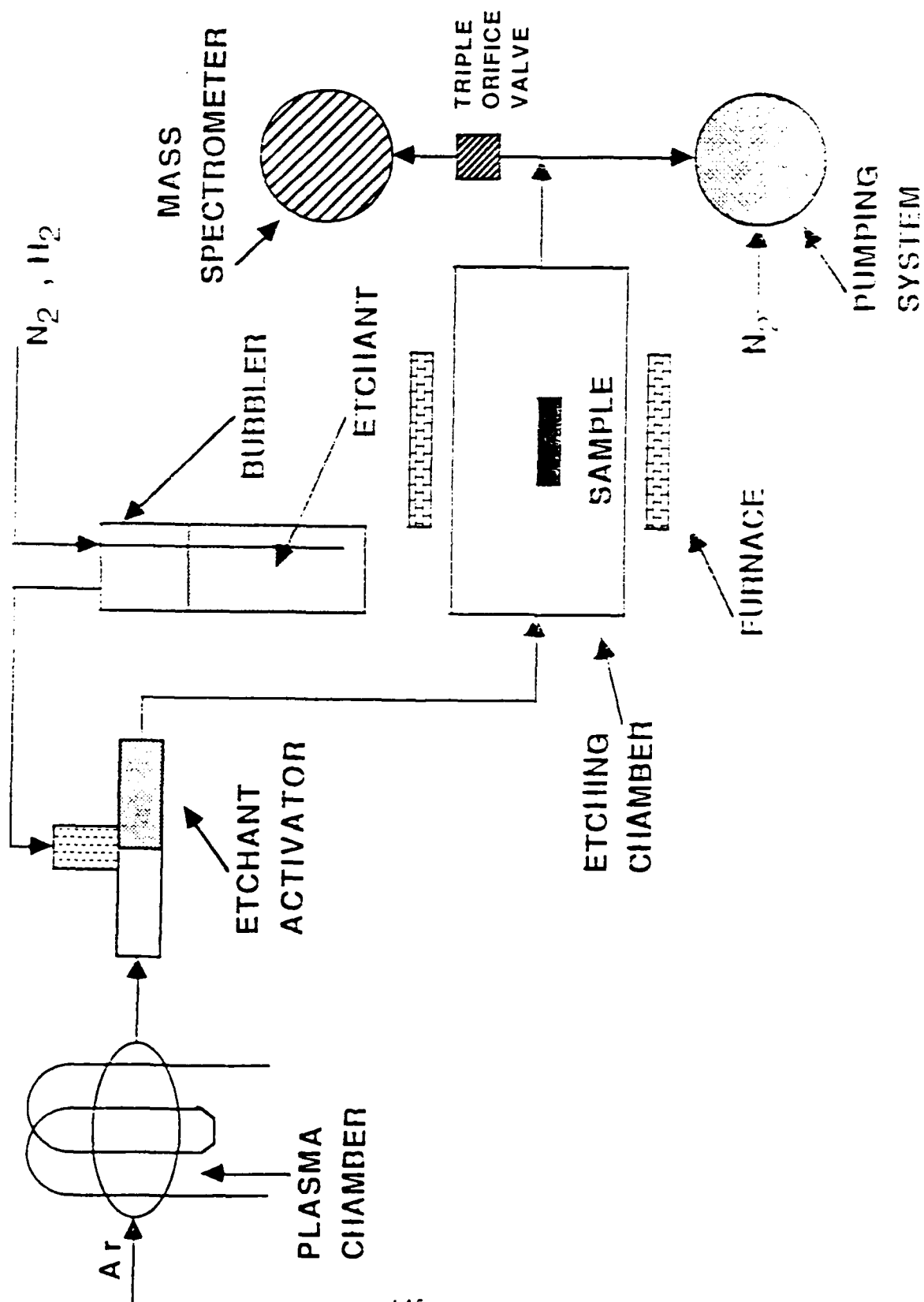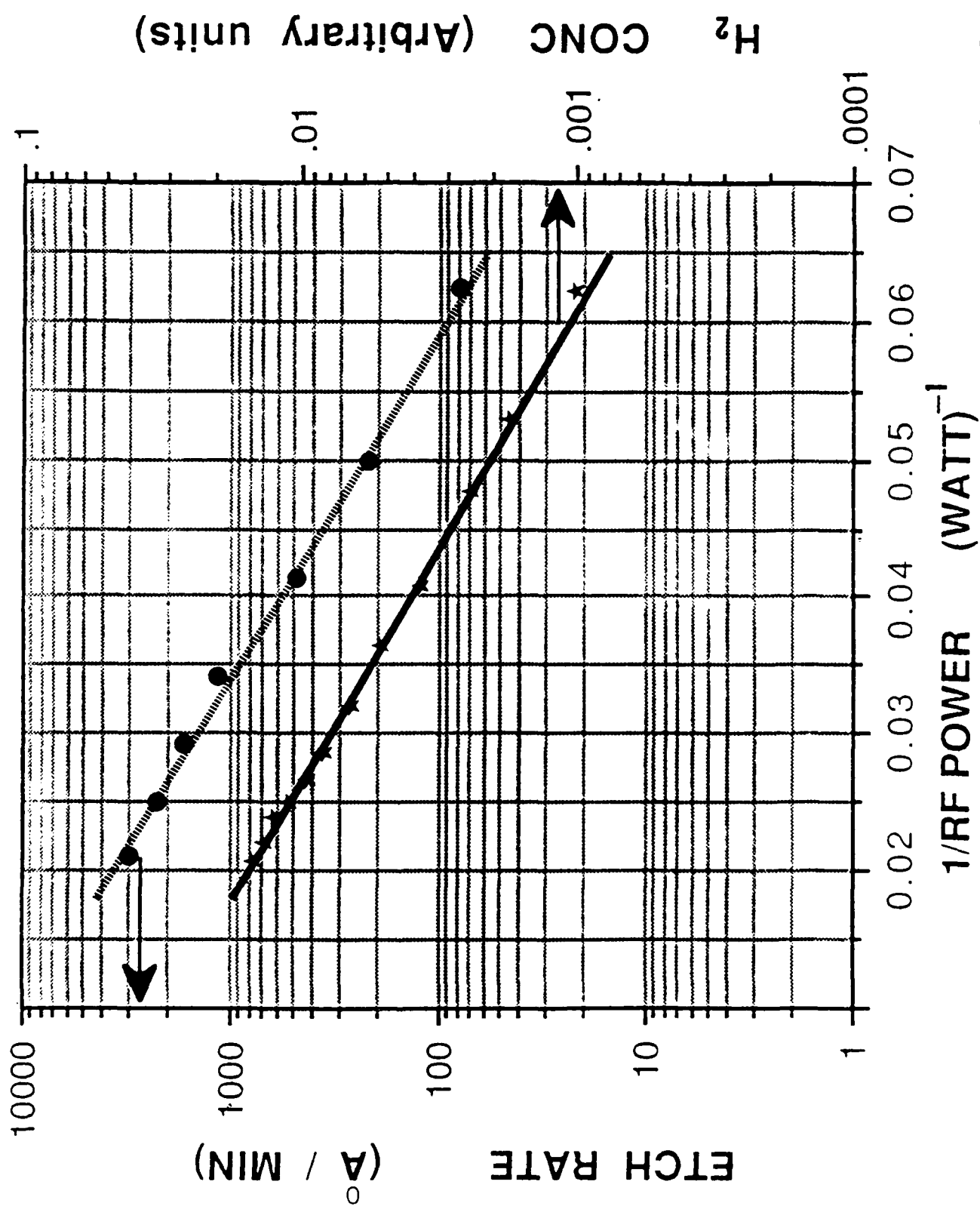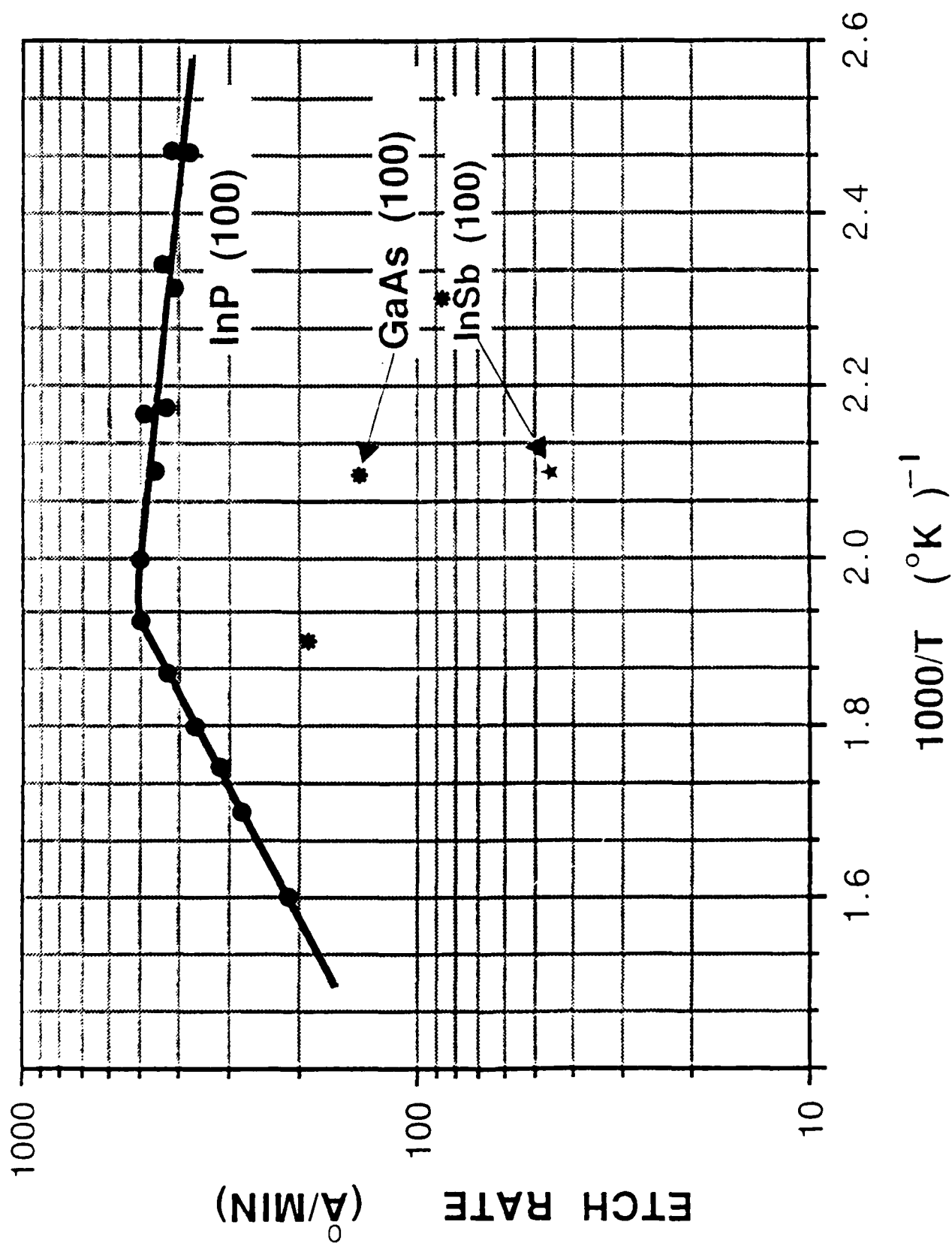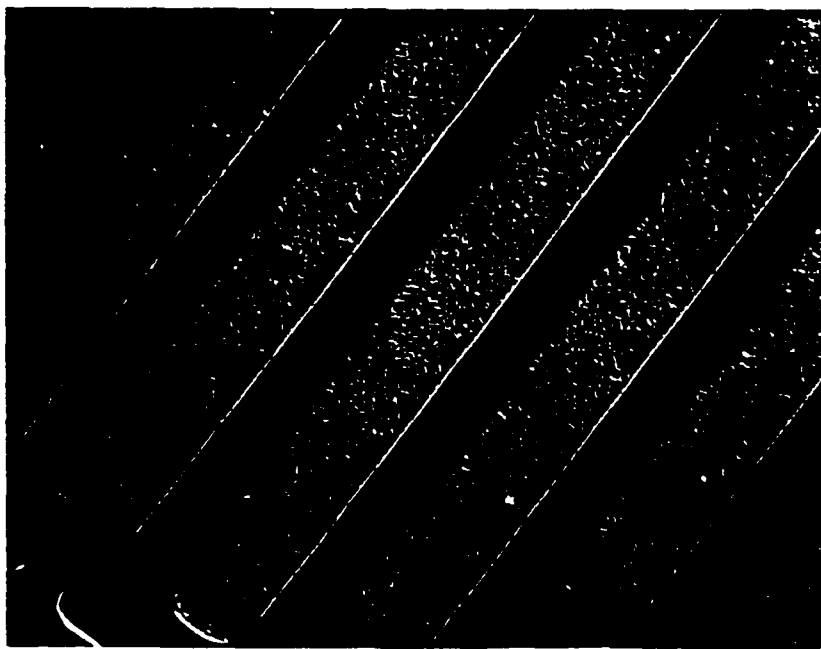*DOWNSTREAM PLASMA ACTIVATED ETCHING OF III-V COMPOUND SEMICONDUCTORS*
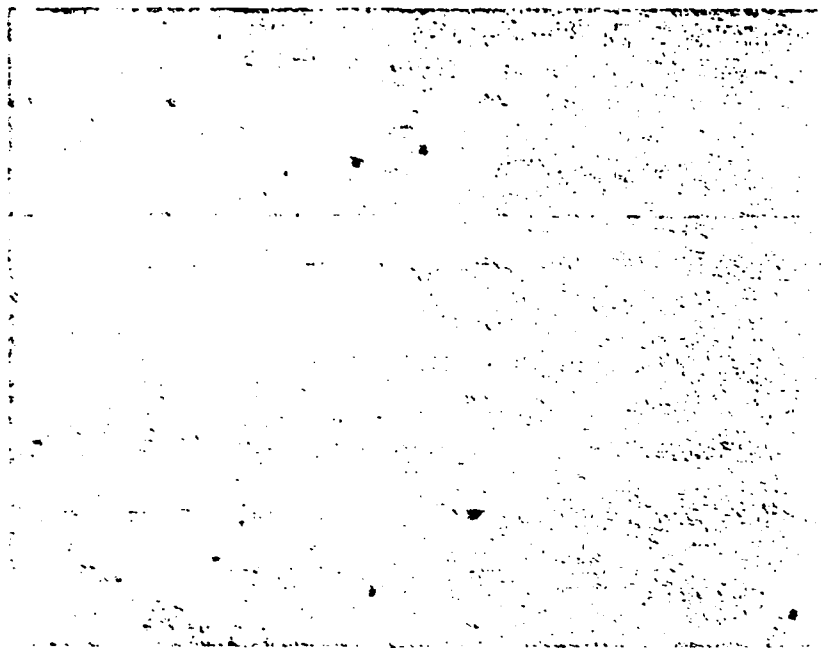
R. Iyer and D. L. Lile

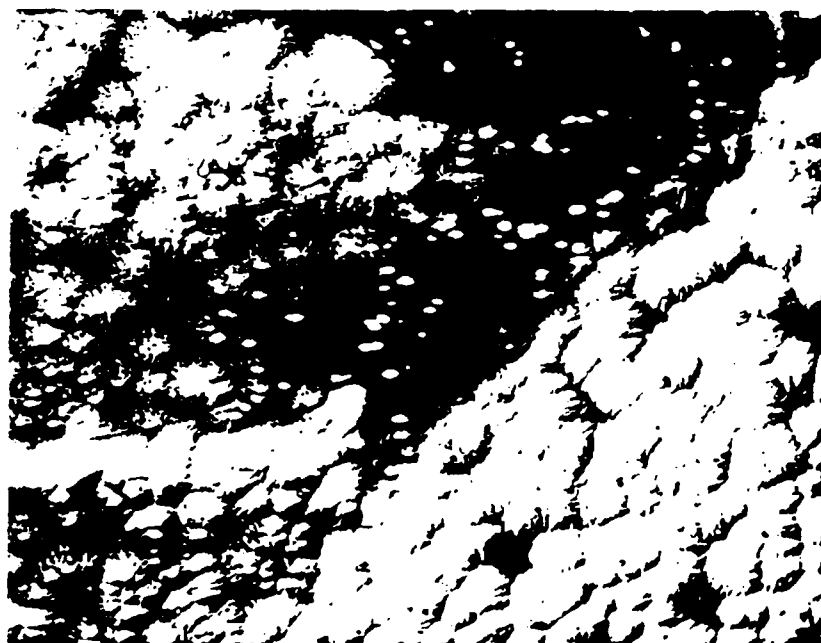*Colorado State University*
Fort Collins, CO

1μm 29.0kV 200E4 0376/00 INP

EXPOSURE TO AIR AFTER ETCHING

H_2/EDB , 22 watts

N_2/EDB
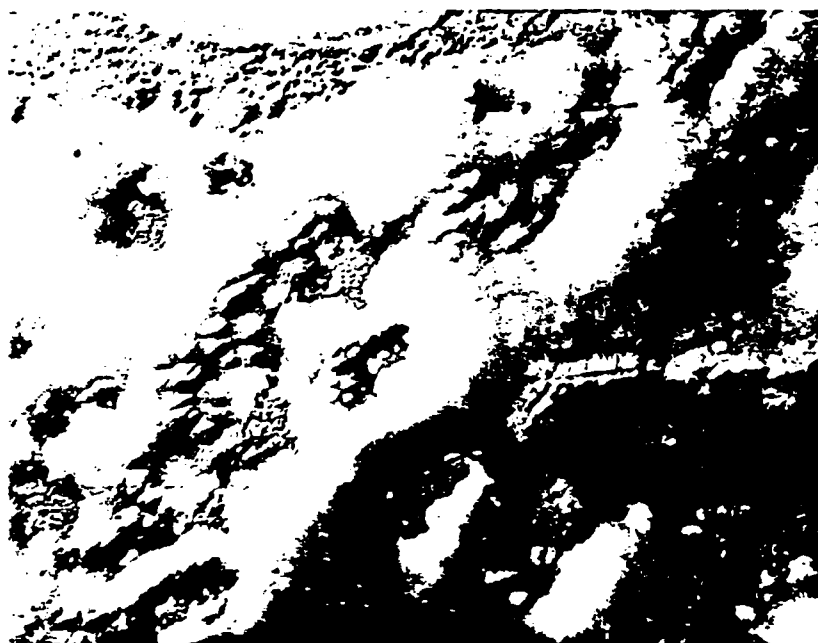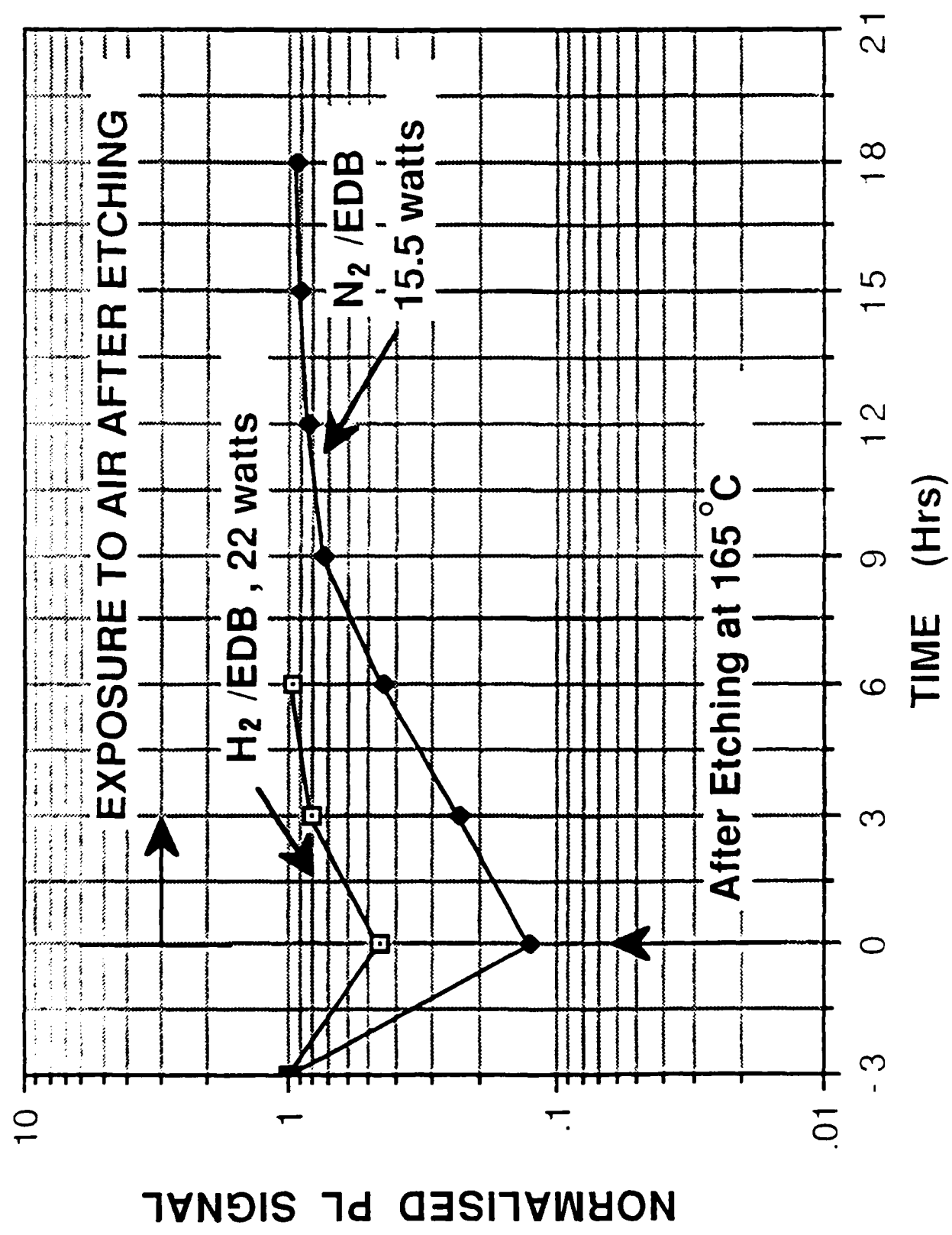15.5 watts

After Etching at 165°C

NORMALISED PL SIGNAL

TIME (Hrs)

AlInAs-GaInAs HBTS FOR HIGH SPEED APPLICATIONS

U. K. Mishra*, A. S. Brown**, and J. F. Jensen

Hughes Research Laboratories
Malibu, CA 90265

*Now at North Carolina State, Raleigh, NC
**Now at Army Research Office, Durham, NC

AlInAs-GaInAs

HBTs FOR HIGH SPEED APPLICATIONS

U.K. Mishra[*], A.S. Brown[**], and J.F. Jensen

* Now at N.C. State University, Raleigh, NC

** Now at Army Research Office, Durham, NC

HUGHES

RESEARCH LABORATORIES

AlInAs-GaInAs HBTs

ADVANGTAGES

- EXCELLENT THRESHOLD CONTROL

- COMPATIBLE WITH OTHER OPTO-ELECTRONIC ELEMENTS

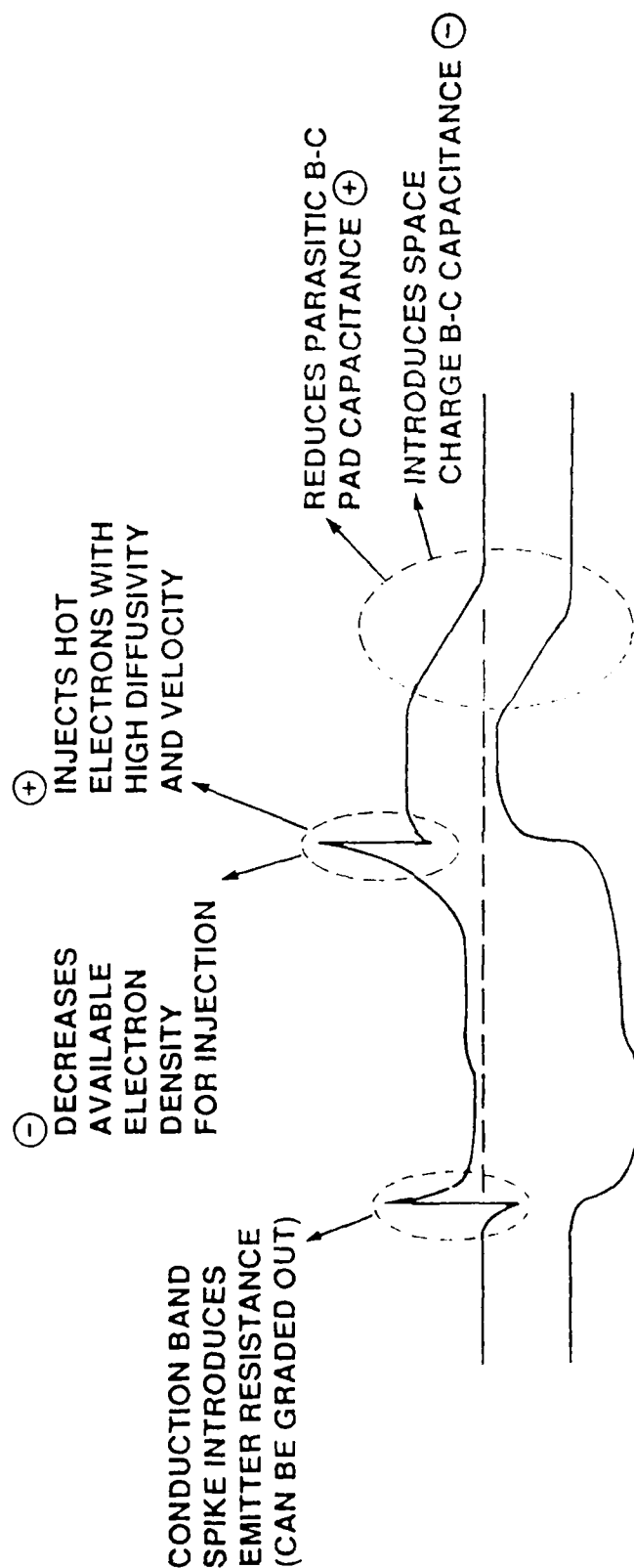- EXCELLENT DRIVE CAPABILITY
  $\Rightarrow$ LOW FAN-OUT SENSITIVITY

DISADVANTAGES

- LOW COLLECTOR BREAKDOWN

- DIFFICULTY IN GROWING AlInAs

- LARGE NUMBER OF PROCESSING STEPS

- VERTICAL DEVICES $\Rightarrow$ HIGH PARASITICS

UM/3 17 89

ADVANTAGES OF AlInAs/GaInAs HBT COMPARED TO AlGaAs/GaAs HBT

- Larger Bandgap Difference ⋅⋅ more suppression of hole injection (Graded Emitter)

- Larger Conduction Band Discontinuity → Higher Electron Injection Velocity (Abrupt Emitter)

- Smaller Base-Emitter Voltage → Lower Power Dissipation

- Larger Γ-L Separation → Higher Velocity → Shorter Transit Time

- Higher Mobility → Lower Parasitic Resistances

SALIENT FEATURES OF CHOSEN HBT DESIGN

(-) DECREASES AVAILABLE ELECTRON DENSITY FOR INJECTION

(+) INJECTS HOT ELECTRONS WITH HIGH DIFFUSIVITY AND VELOCITY

REDUCES PARASITIC B-C PAD CAPACITANCE (+)

INTRODUCES SPACE CHARGE B-C CAPACITANCE (-)

CONDUCTION BAND SPIKE INTRODUCES EMITTER RESISTANCE (CAN BE GRADED OUT)

n··	n·	n	p·	u	n··
InGaAs .53 .47	AlInAs .48 .52	AlInAs .48 .52	InGaAs .53 .47	InGaAs .53 .47	InGaAs .53 .47

EMITTER BASE COLLECTOR

$$f_T = \frac{1}{2\pi\tau_{eC}}$$

$$\tau_{eC} = \tau_e + \tau_b + \tau_C$$

$$\left(R_E C_E + R_E C_{BC}\right) + \frac{W_B^2}{\eta D_B} + \frac{x_C}{2V_{av}}$$

$$f_{max} \cong \frac{1}{4\pi\left[R_B C_{BC}\tau_{eC}\right]^{1/2}}$$

$$C_E \downarrow, \; C_{BC} \downarrow, \; R_B \downarrow, \; V_{av} \uparrow; \; W_B \downarrow, \; R_E \cdot \left[\frac{kT}{qI_C} \cdots I_C \uparrow\right]$$
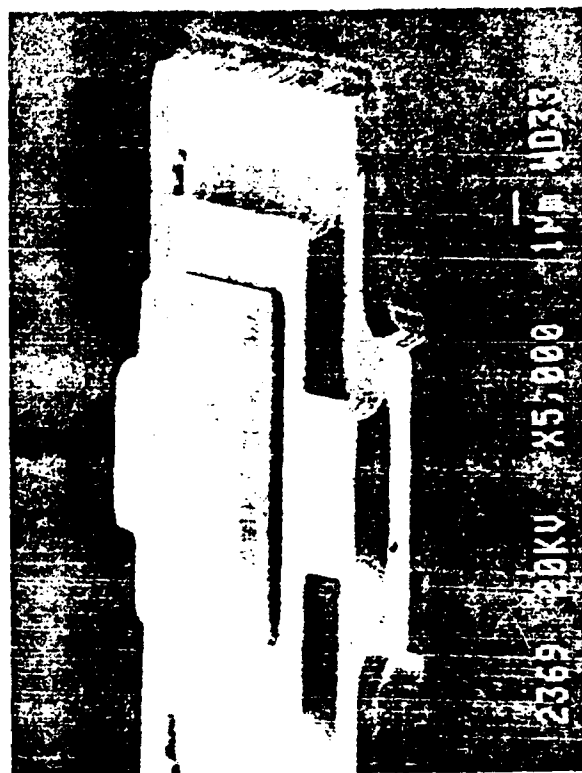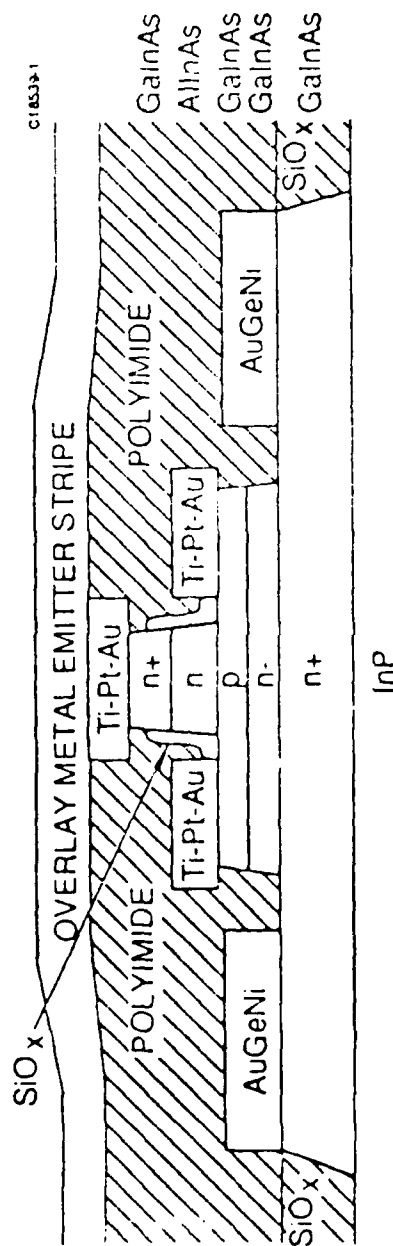
HBT PROCESS OUTLINE

PROCESS STEP

1. Grow AllnAs-GaInAs HBT device material

2. Define emitter ohmic contact metal

3. Etch emitter mesa down to base

4. Form SiO_2 sidewall

5. Define base ohmic contact metal

6. Etch base mesa down to sub-collector

7. Etch collector mesa and SiO refill - device isolation

8. Define collector ohmic metal

9. Planarize to emitter surface

10. Etch vias

11. Define overlay metal

JJ/10-31
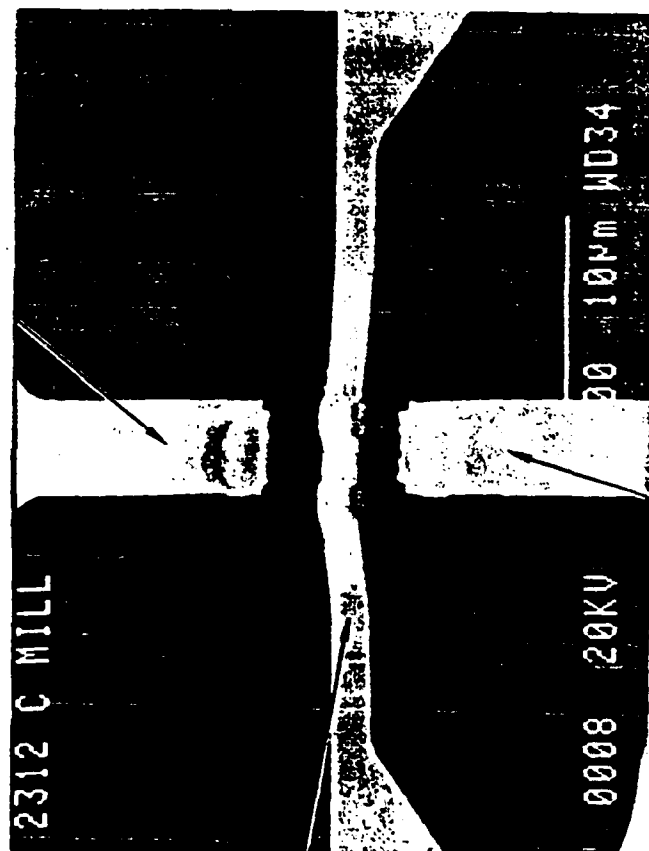
160

AllnAs/GaInAs
WET ETCH HBT PROCESS

HUGHES

8852-01-01

C18531

OVERLAY METAL EMITTER STRIPE

SiOx

POLYIMIDE

POLYIMIDE

AuGeNi

Ti-Pt-Au

Ti-Pt-Au

Ti-Pt-Au

n+

n

p

n-

n+

InP

SiOx

GaInAs
AlInAs
GaInAs
GaInAs
SiOx GaInAs

2369 20KV X5,800 1μm WD33

OCT 1988

AlInAs/GaInAs HBT DEVICE

HUGHES

COLLECTOR

EMITTER

BASE

2 μm by 3 μm DOUBLE EMITTER DEVICE

2312 C MILL

0008 20KU 10μm WD34

C18385 6

AUGUST 1988

HUGHES

8852 01 04

AlInAs/GaInAs
BREAKDOWN CHARACTERISTICS
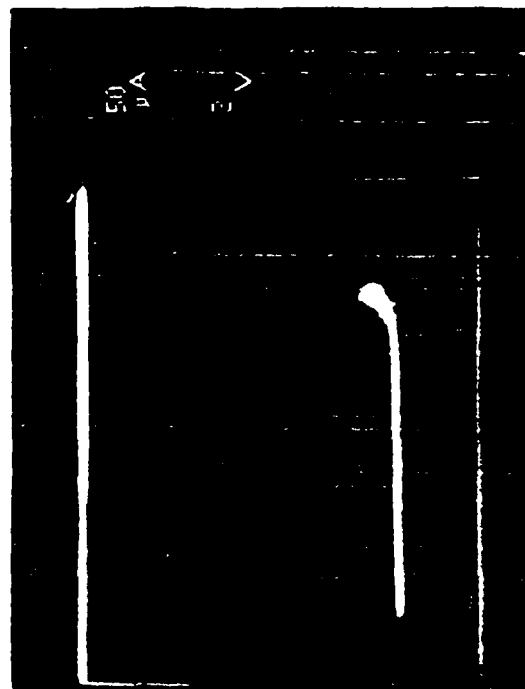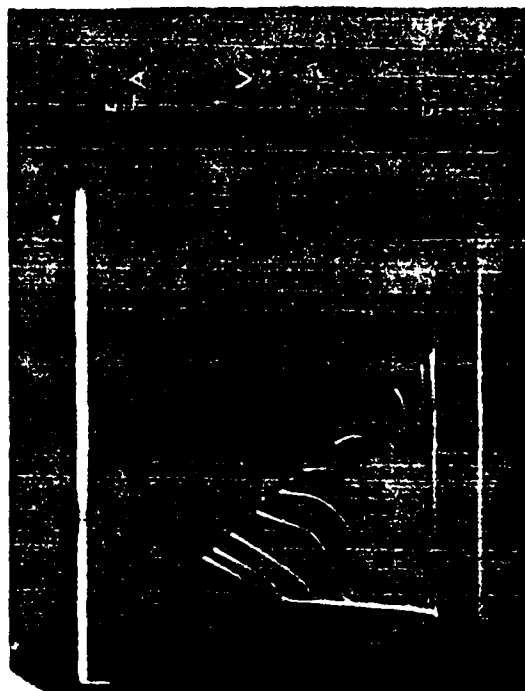
BVCEO=4 V

BVCBO=17 V
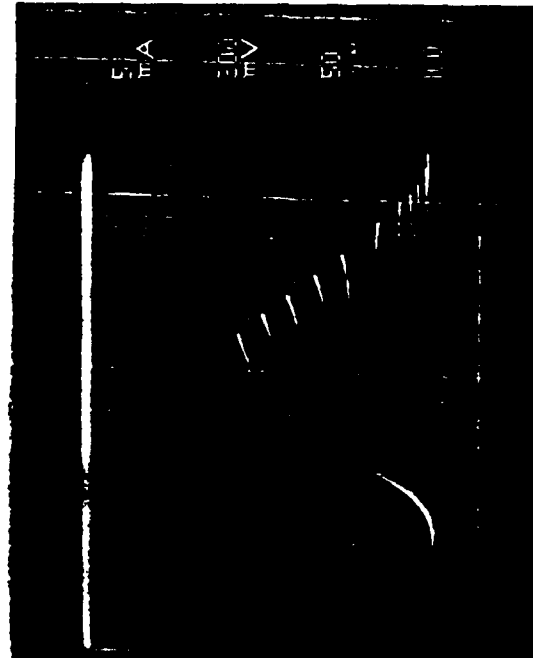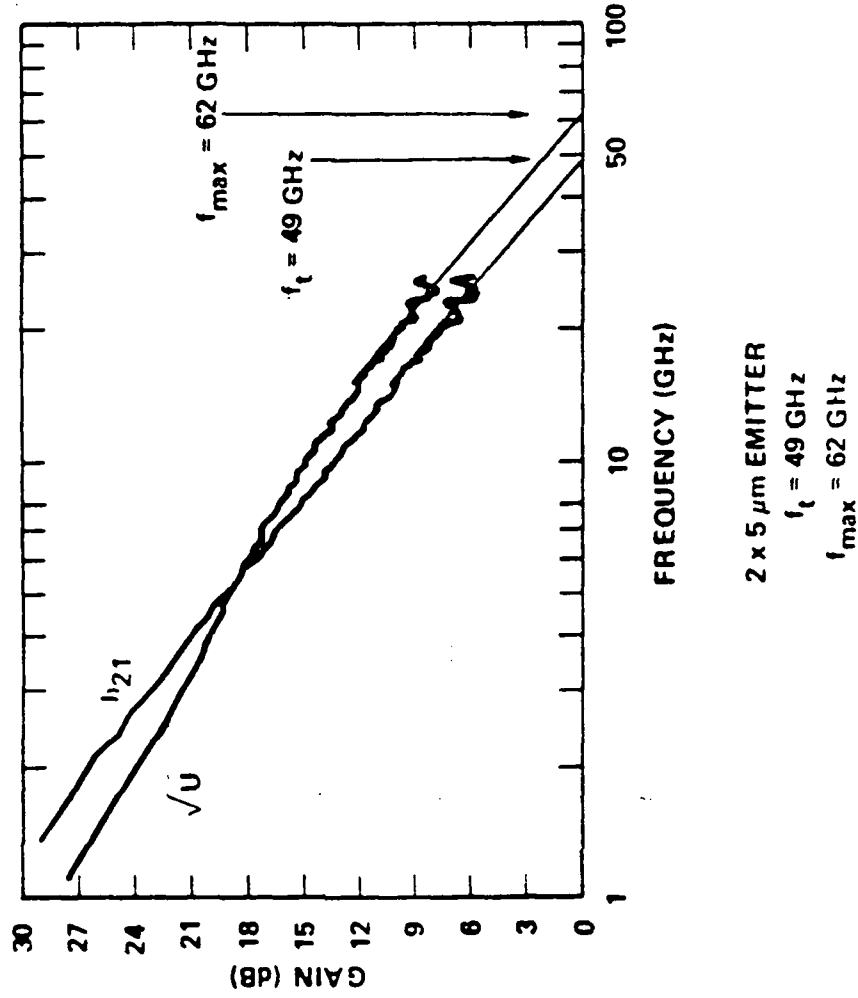
OCT 1988

AlInAs / GaInAs HBT f_t, f_{max} and β VERSUS
COLLECTOR CURRENT 2 x 5 μm EMITTER

COLLECTOR CURRENT ma

f_t, f_{max}

β
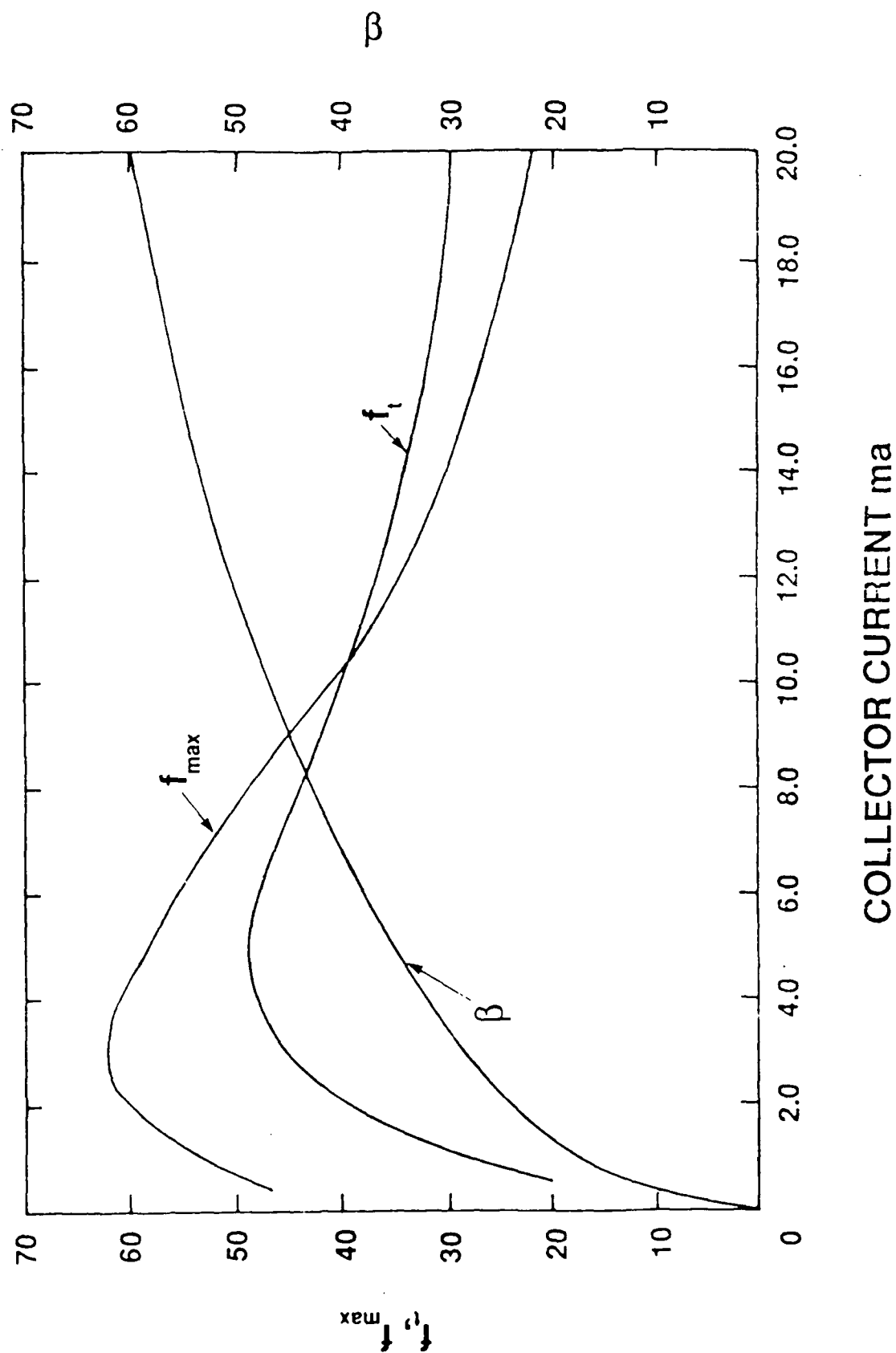
AlInAs/GaInAs HBT f_t AND f_{max} VERSUS

COLLECTOR CURRENT 2 x 5 μm EMITTER

8852–01–02

f_{max}

f_t

f_t, f_{max}

COLLECTOR CURRENT ma

70 60 50 40 30 20 10 0

0   2.0   4.0   6.0   8.0   10.0   12.0   14.0   16.0   18.0   20.0

OCT 1988

166
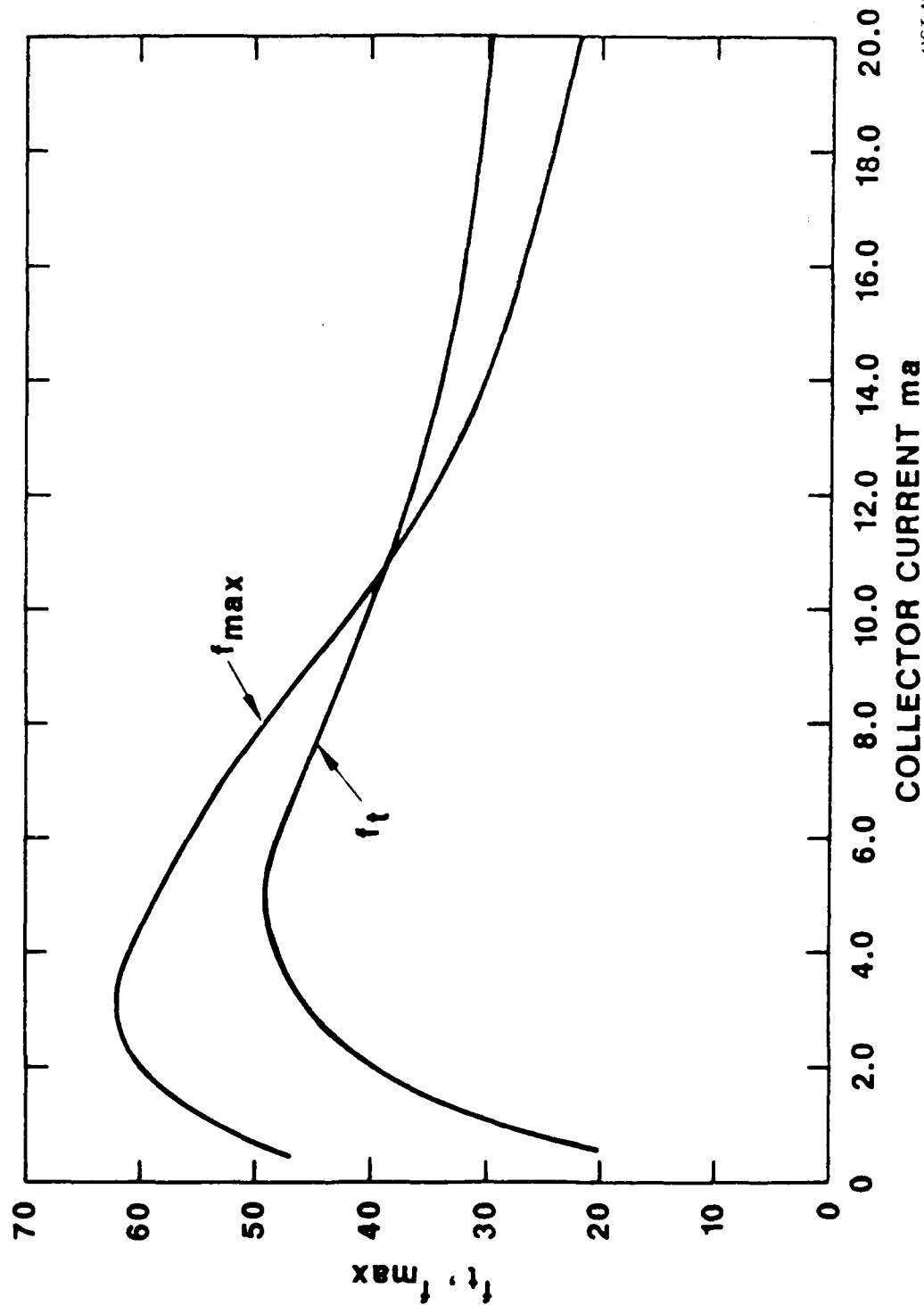
EFFECT OF UNDOPED COLLECTOR ON f_T & f_{max}

⊖ $v_B \uparrow$

NEGLECTING SPACE CHARGE

WITH SPACE CHARGE
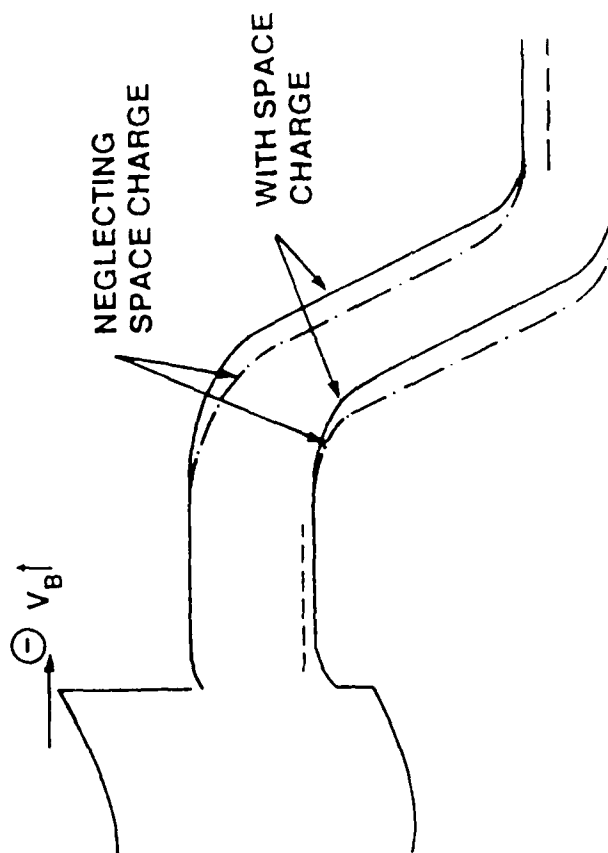
- $J_c \uparrow \Rightarrow n_c \uparrow$
- $n_c \uparrow \Rightarrow \varepsilon \downarrow \Rightarrow V_c \downarrow$
- $n_c \uparrow \Rightarrow \tau_c \uparrow \Rightarrow C_{bc} \uparrow$

$\tau_c \uparrow, C_{bc} \uparrow \Rightarrow f_T \downarrow, f_{max} \downarrow$

$$\alpha = \frac{\alpha_0 e^{-j\omega\tau}}{1 + j\, f/f_\alpha}$$

C_{BC} R_{BC} αI_E R_C

R_B C_{BE} R_E

R_{BE}

R_{B1} C_s

168

Base-Emitter Junction Ideality Factor, n vs Collector Current, mA

170

Cbe

Rbe

Cbc
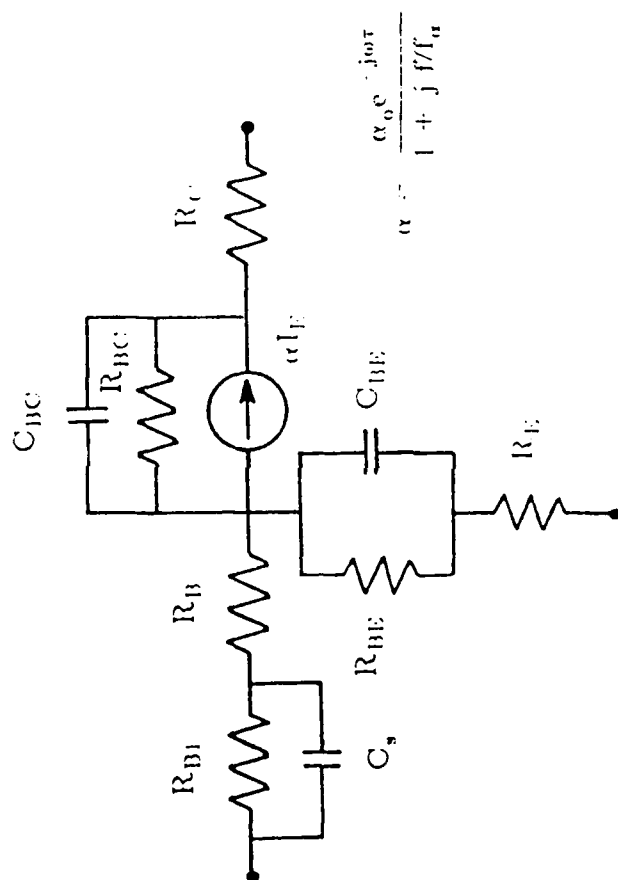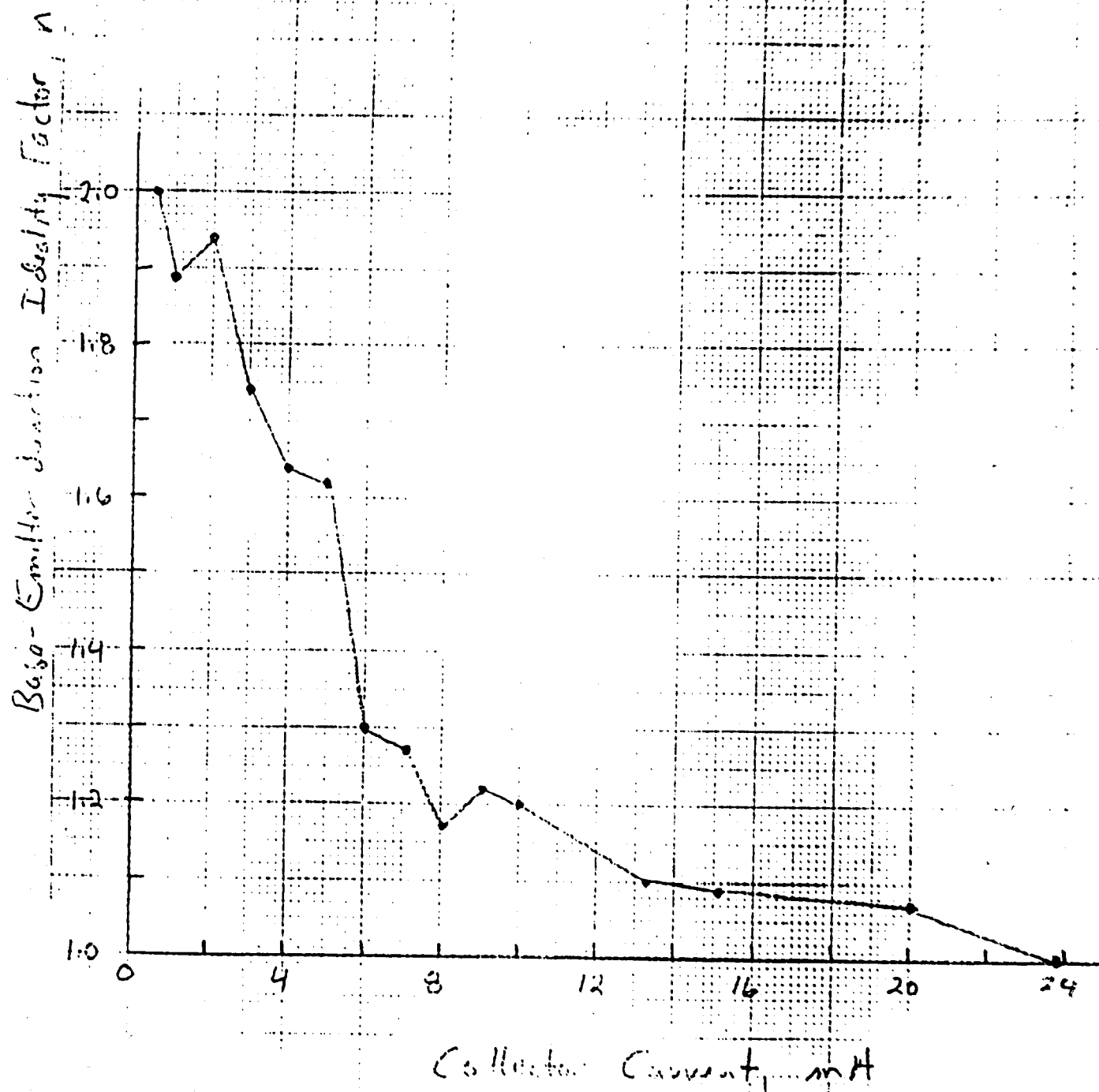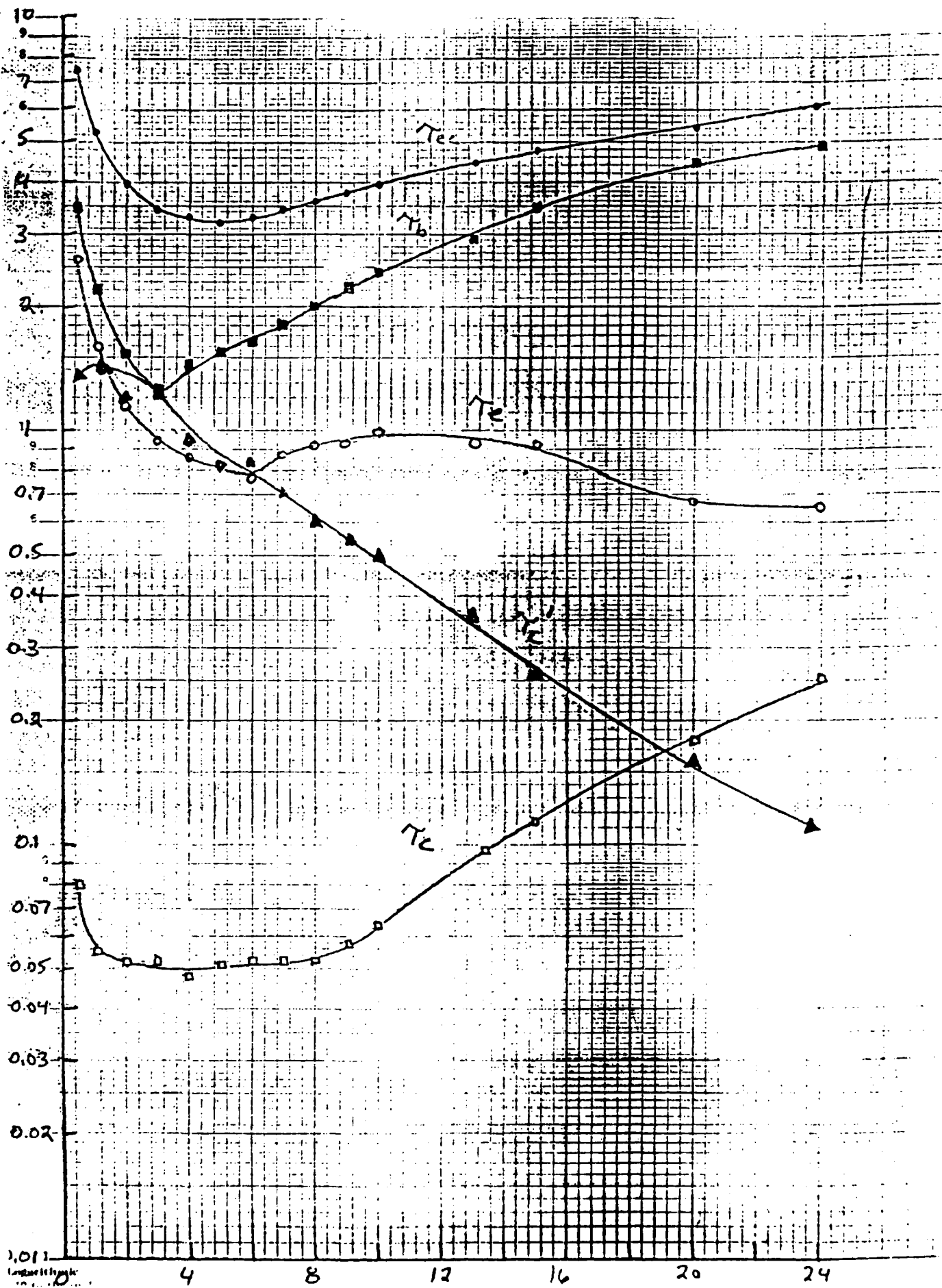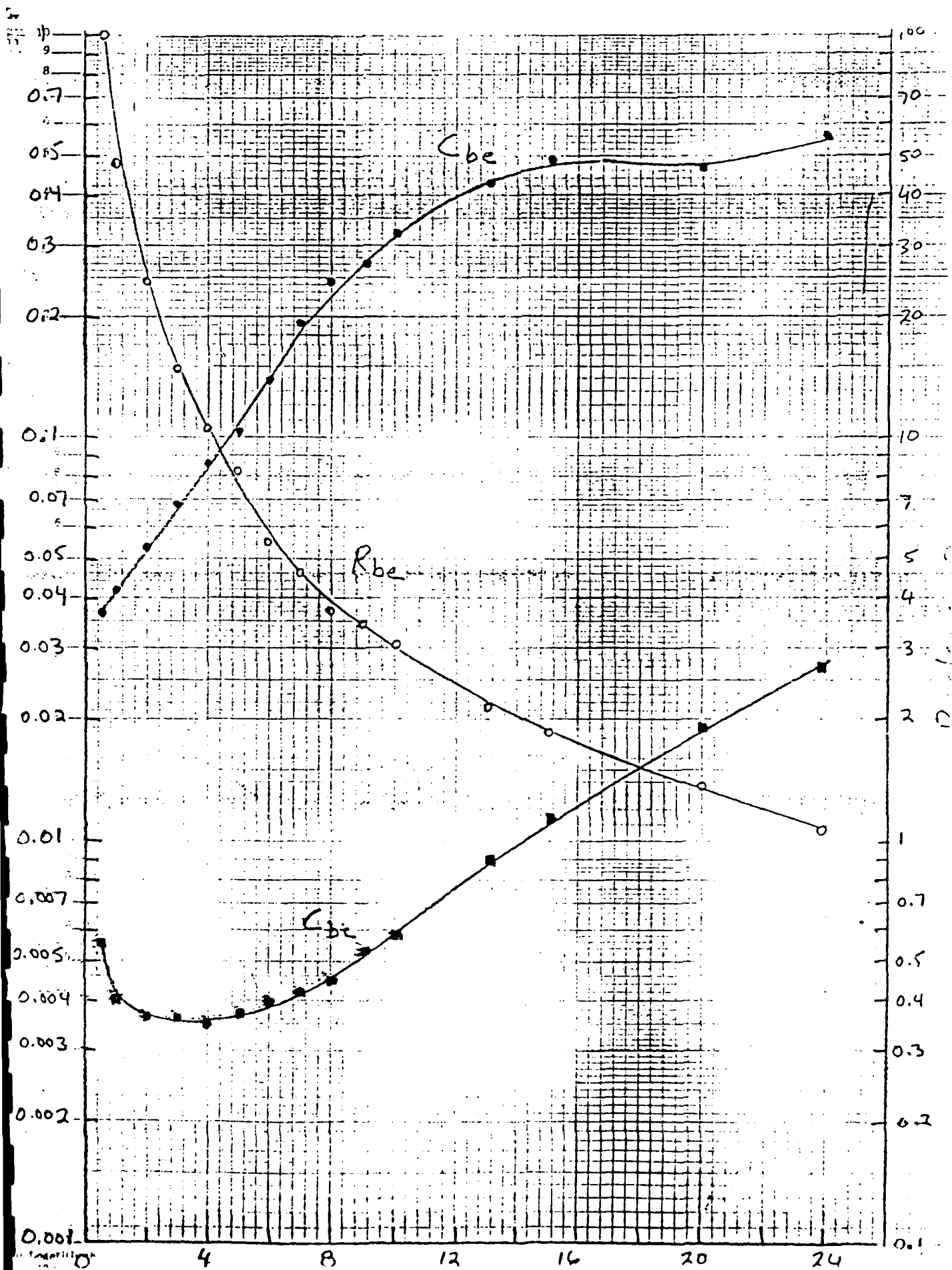
CONCLUSIONS

- AllnAs-GaInAs HBTs have been fabricated with excellent high frequency performance $\left(f_T = 48\text{GHz} \; f_{max} = 62\text{GHz} \right)$.

- Limits to performance have been related to epitaxial layer design.

- Improved collector layer design will result in high f_T and f_{max}.

- Improved base layer design will result in high f_{max}.

HIGH PERFORMANCE In,GaAs MODFETS ON InP AND GaAs

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Ithaca, NY 14853

HIGH PERFORMANCE In,GaAs MODFET'S ON InP AND GaAs

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A comparison is made between high frequency performance of $In_xGa_{1-x}As$/GaAs and $In_{.53}Ga_{.47}As$/InP MODFET's. The best f_T value for the former's is 150 GHz for .14 μm gate devices, and for the latter is 170 GHz for .10 μm gate devices. Average electron transit velocity, in different MODFET's, and other important parameters will be covered.

COMPOUND SEMICONDUCTOR DEVICE FUTURE HIGH

FREQUENCY TECHNOLOGIES FOR KEY APPLICATIONS

Low Noise Receivers:

<u>MODFETS</u>
1. Al,InAs/GaInAs/InP, (or/GaAs-MISFIT)
2. AlGaAs/GaInAs/GaAs Strained-pseudomorphic
3. AlGaAs/GaAs
<u>MESFETS:</u>
1. GaInAs
2. GaAs

High Power Transmitters
1. InP MISFET
2. AlGaAs/GaInAs/GaAs HBT
3. GaAs PBT
4. AlGaAs/GaInAs/GaAs MODFET
5. GaAs MESFET

Logic
1. AlGaAs/GaInAs/GaAs HBT
2. AlGaAs/GaInAs/GaAs MODFET
3. GaAs MESFET

COMPARISON OF ELECTRON AVERAGE TRANSIT VELOCITY IN FET's

DOPED CHANNELS

   GaAs - 1.0 x 10^7cm/s
   InP ~ 1.6 x 10^7cm/s

UNDOPED CHANNELS - 2 DEG's

   GaAs substrates and $Al_{.3}Ga_{.7}As$ doped barriers
      GaAs - 1.2 x 10^7cm/s
      $In_{.15}Ga_{.85}As$ - 1.5 x 10^7cm/s
      $In_{.25}Ga_{.75}As$ - 1.8 x 10^7cm/s

   InP substrates and $Al_{.48}In_{.52}As$ doped barriers
      $Ga_{.47}In_{.53}As$ - 2.4 x 10^7cm/s
      $Ga_{.35}In_{.65}As$ ~ 2.6 x 10^7cm/s

THESE VELOCITIES DETERMINE $f_{ti} = v_{eff}/(2\pi L_{g\ eff})$

Gate

3 μm

0.25 μm

Source

Drain

500Å 400Å

n^+ GaAs

300Å n^+ $Al_{0.3}Ga_{0.7}As$

d

undoped $Al_{0.3}Ga_{0.7}As$
spacer layer

GaAs Buffer 1 μm

undoped LEC SI GaAs substrate

In$_x$Ga$_{1-x}$As on GaAs

LIMITED TO MATTHEWS–BLAKESLEE THICKNESS

INDIUM PERCENTAGE in InGaAs SINGLE QW

InGaAs CRITICAL LAYER THICKNESS (Å)
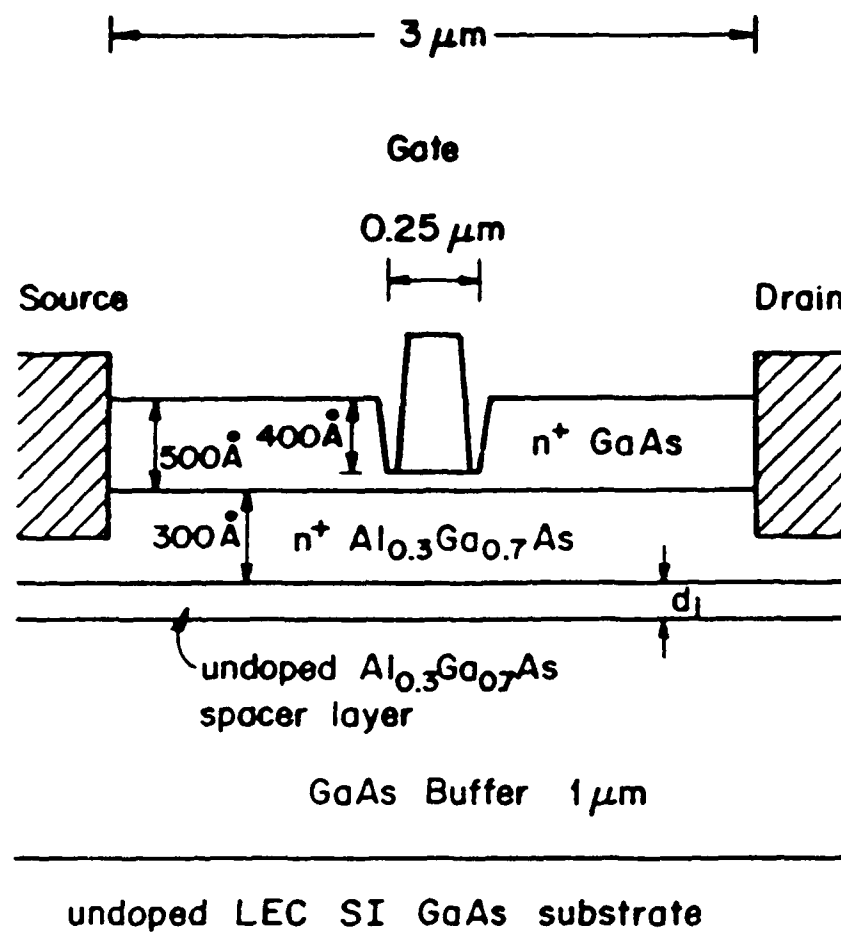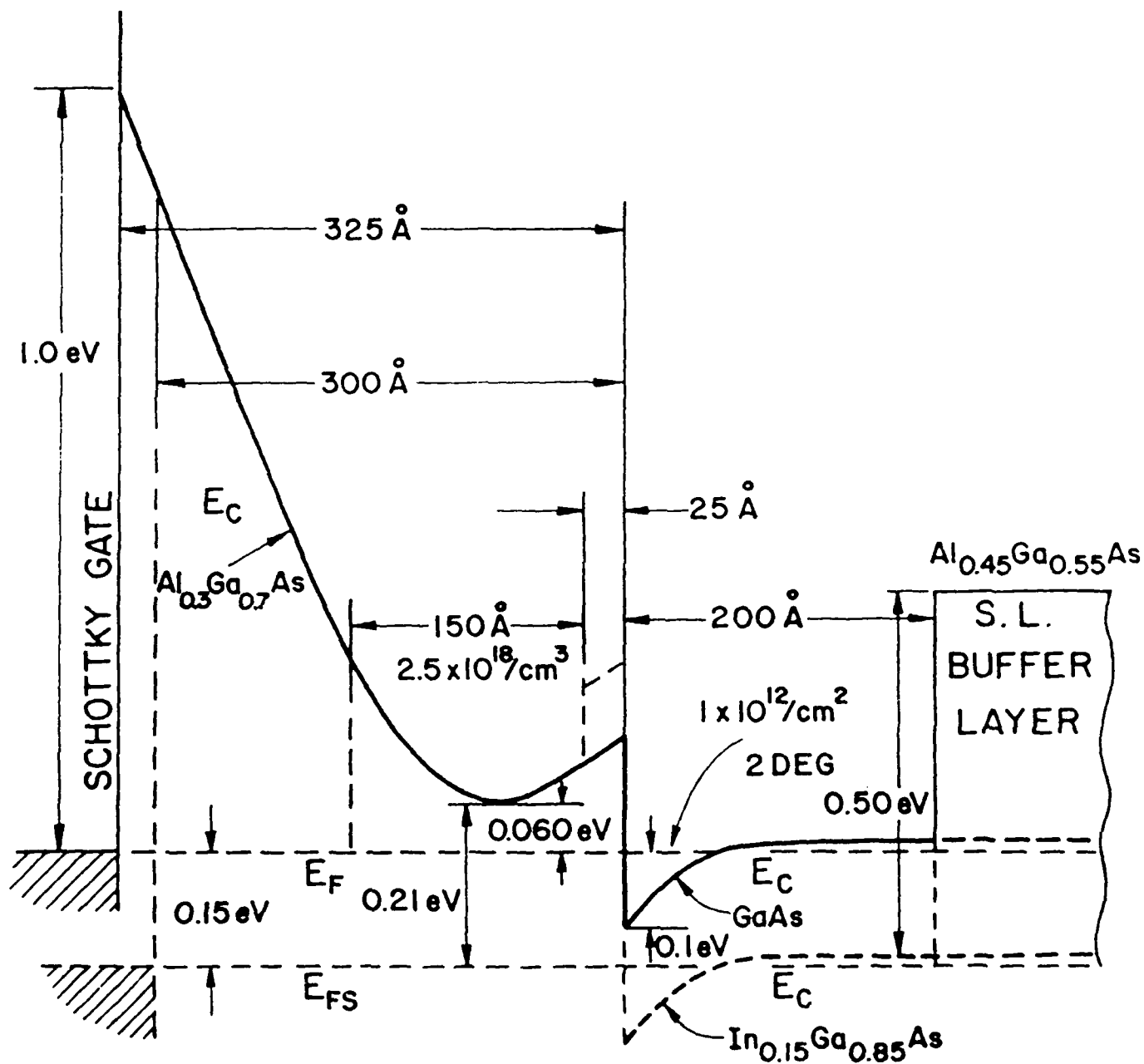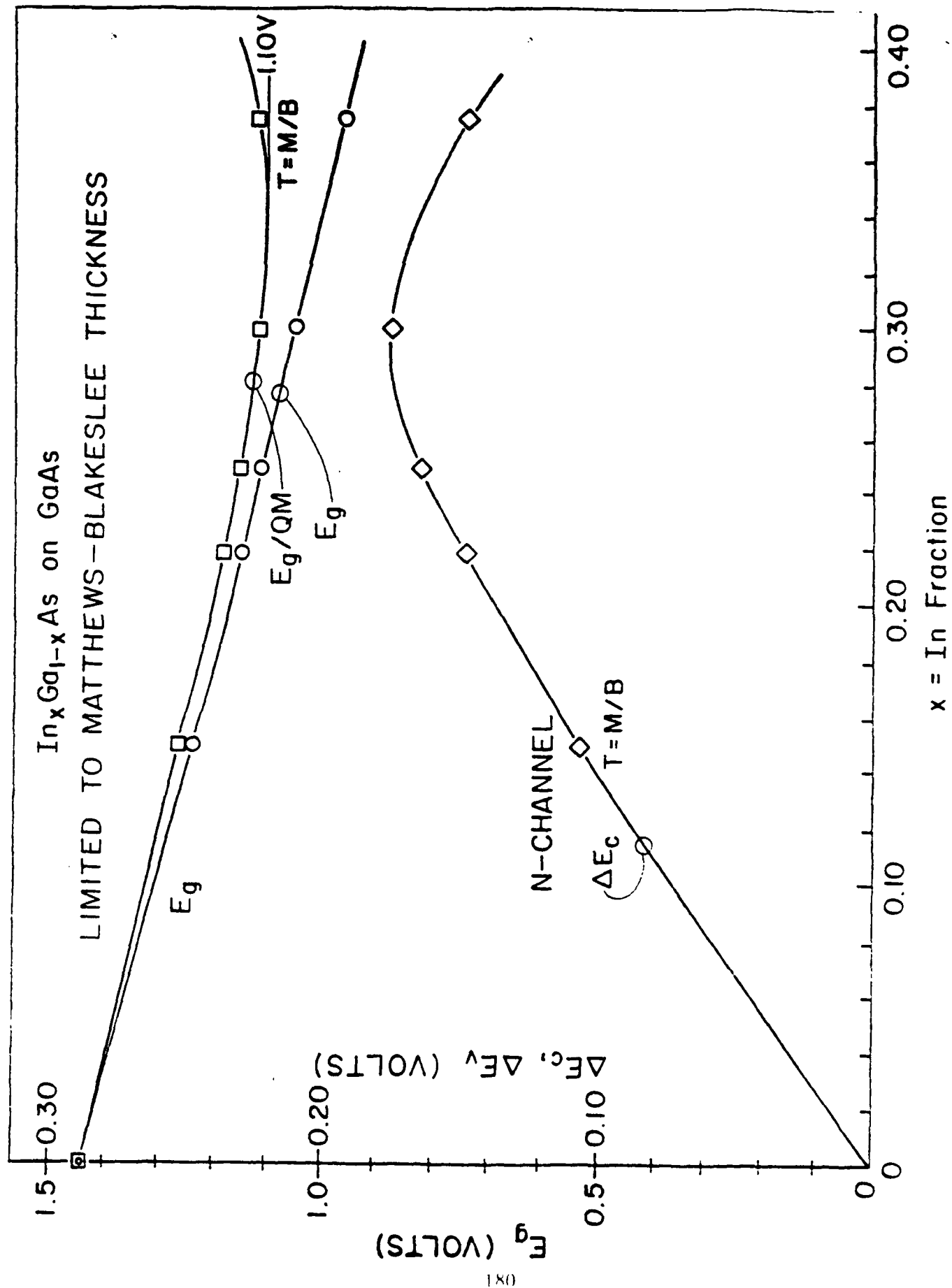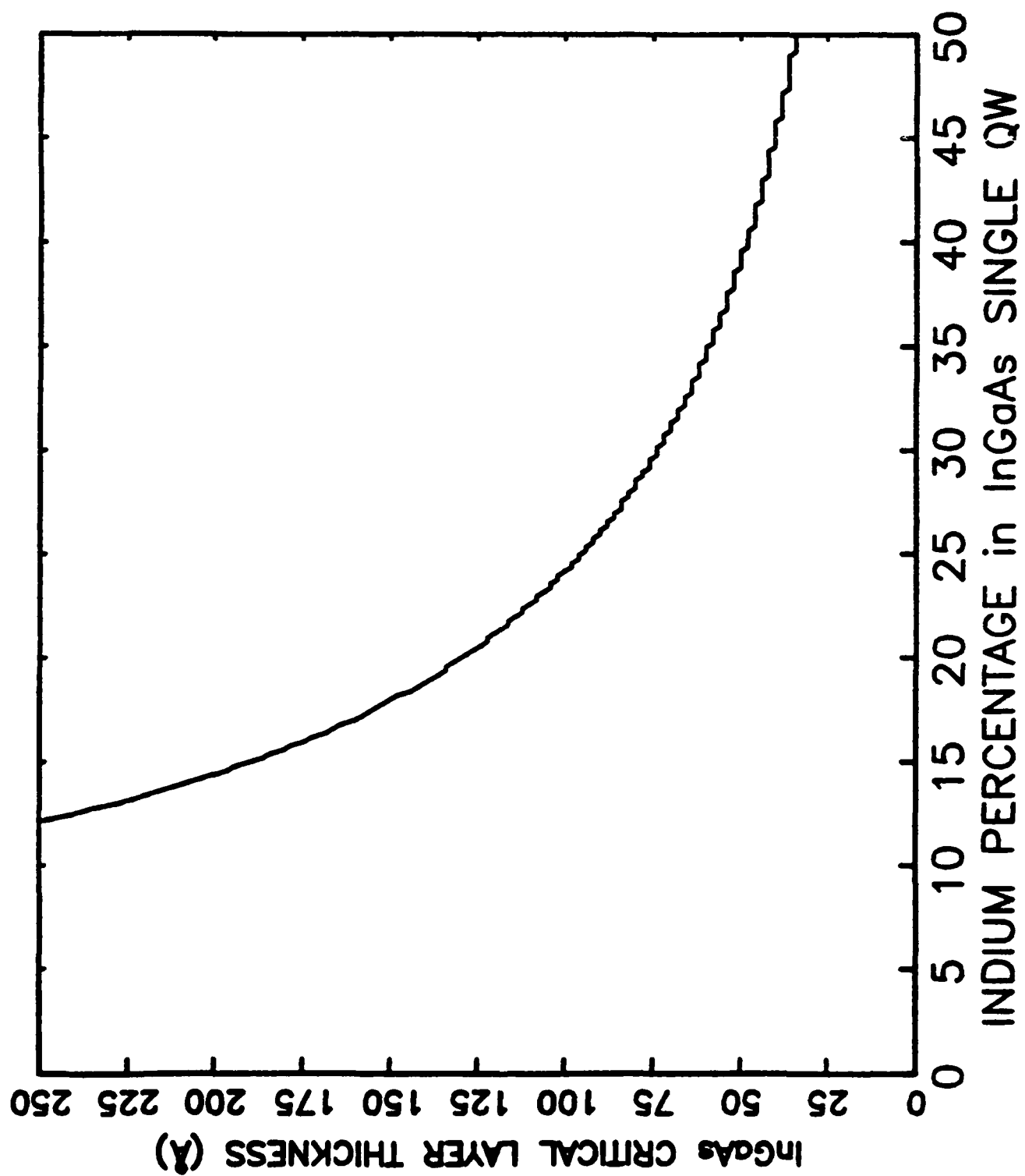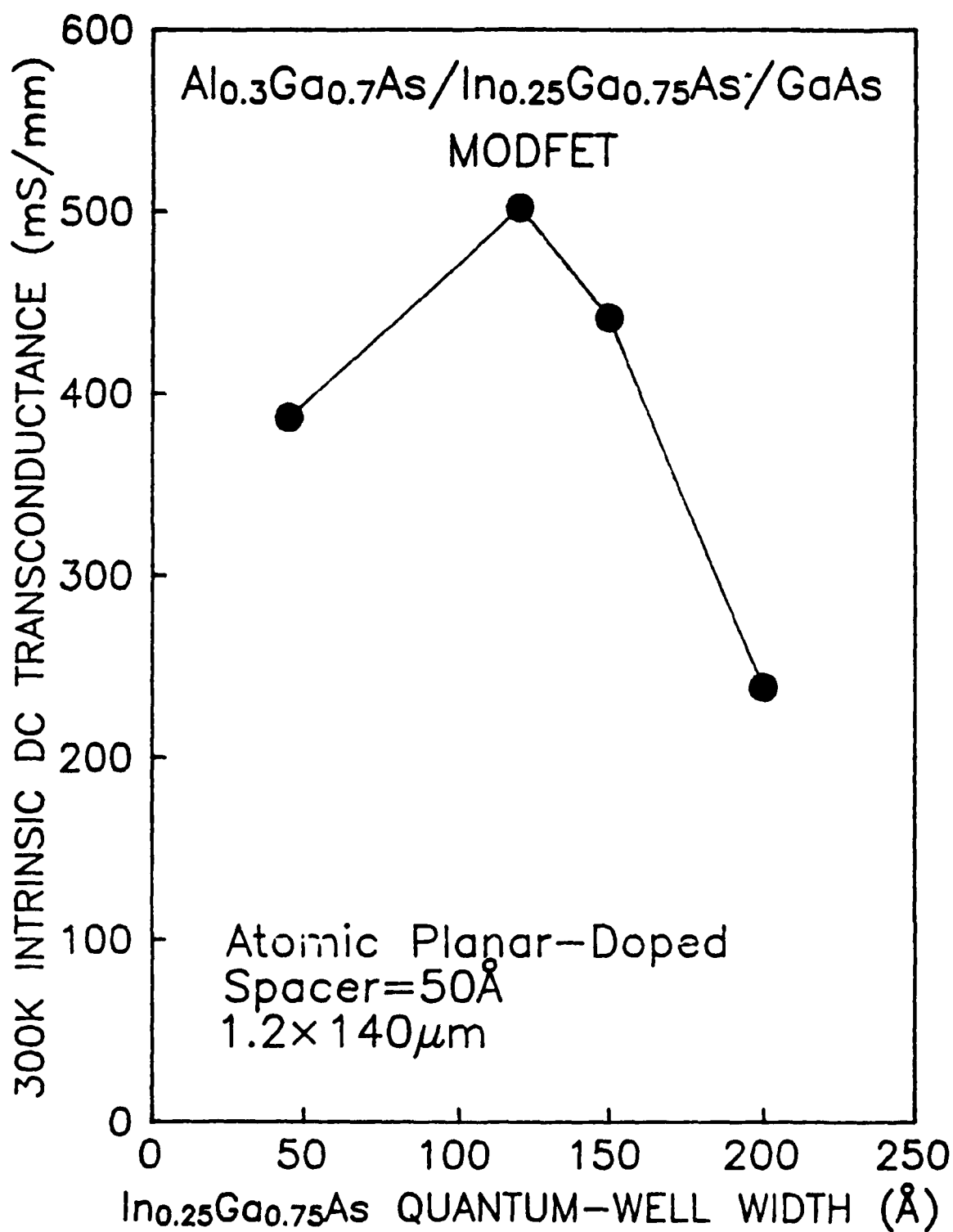
0.15×150μm MUSHROOM GATE InGaAs MODFET

f_T = 152 GHz

V_{DS} = 1.0 V
V_{GS} = 0.05 V
I_{DS} = 237 mA/MM

CURRENT GAIN (dB)
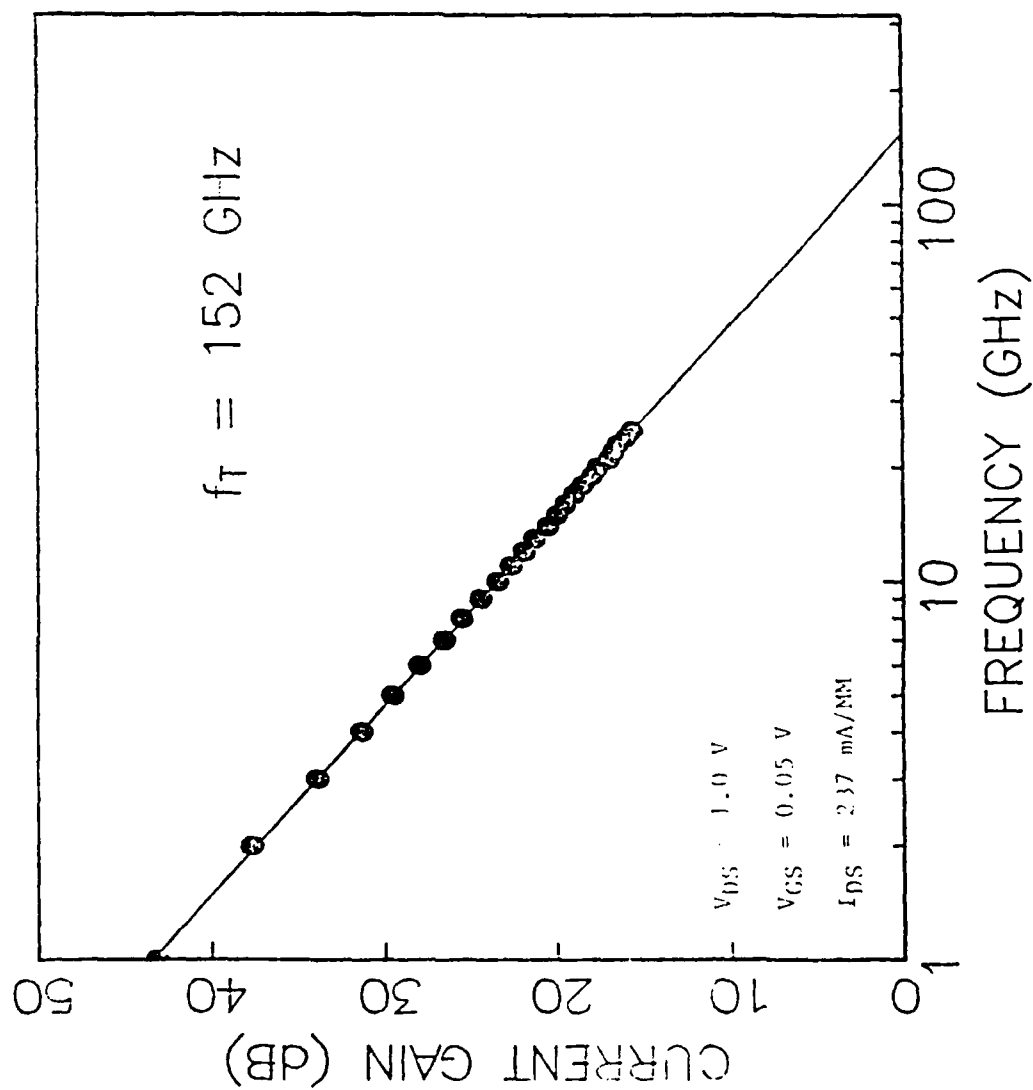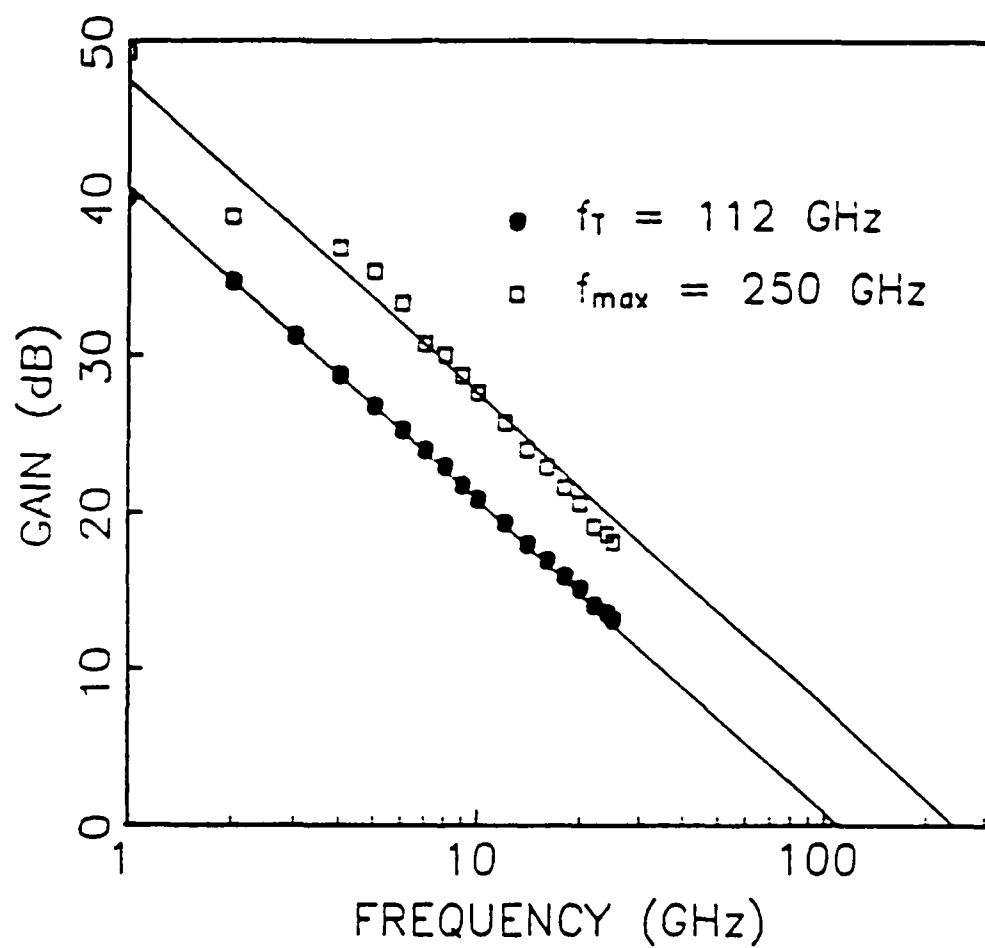
FREQUENCY (GHz)

Current and unilateral gain of a 50 μm wide AlGaAs/InGaAs

MODFET (V_{ds} = 2.0 V, V_{gs} = - 0.05 V, I_{ds} = 14.7 mA)

FABRICATION

★ 25% InGaAs ($v_{eff} = 1.8 \times 10^7$ cm/s)

● 15% InGaAs (1.5×10^7 cm/s)

○ GaAs (1.2×10^7 cm/s)

◐ GaAs APD (1.3×10^7 cm/s)

MATERIAL

CURRENT GAIN CUT-OFF FREQUENCY f_T (GHz)
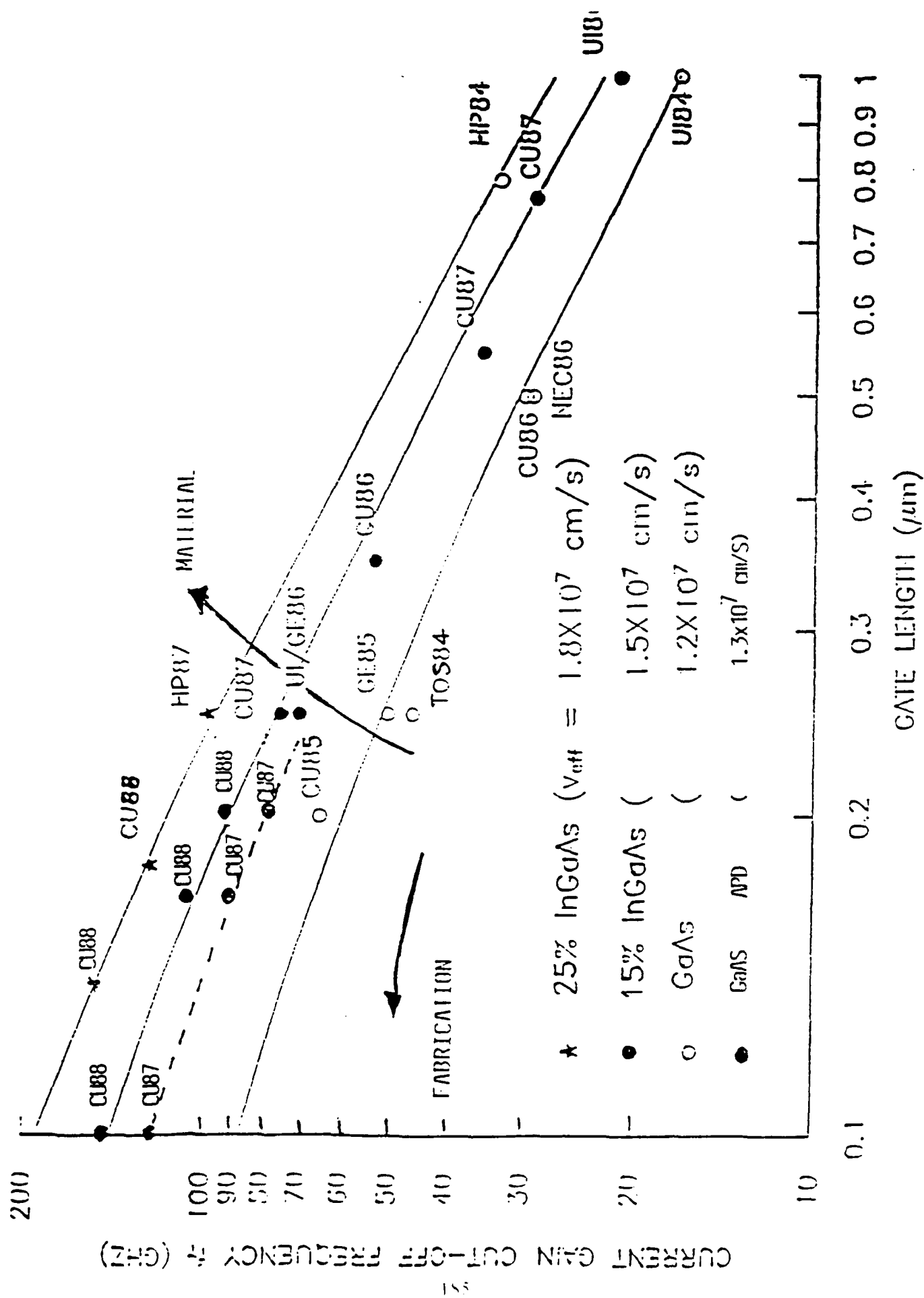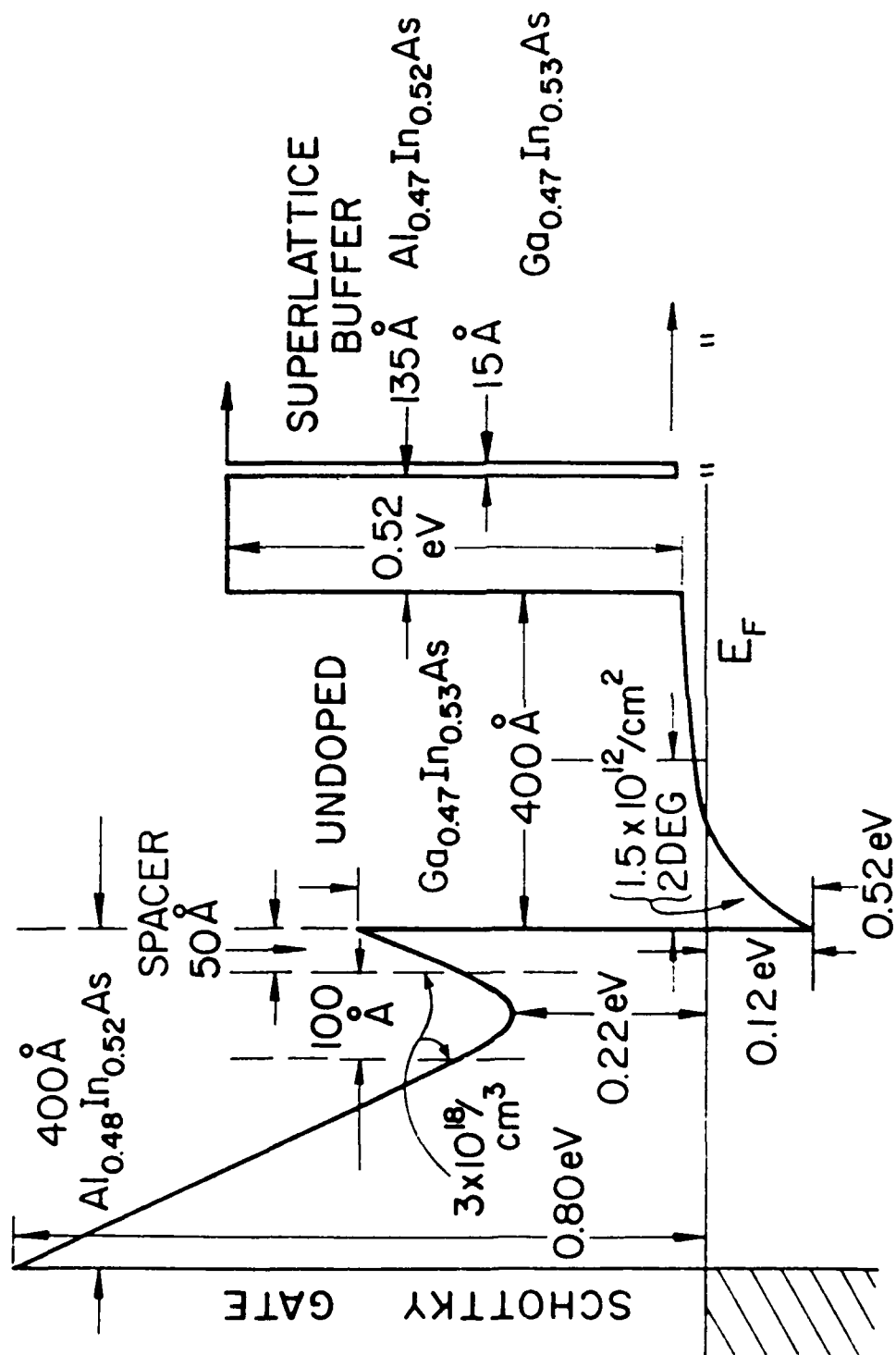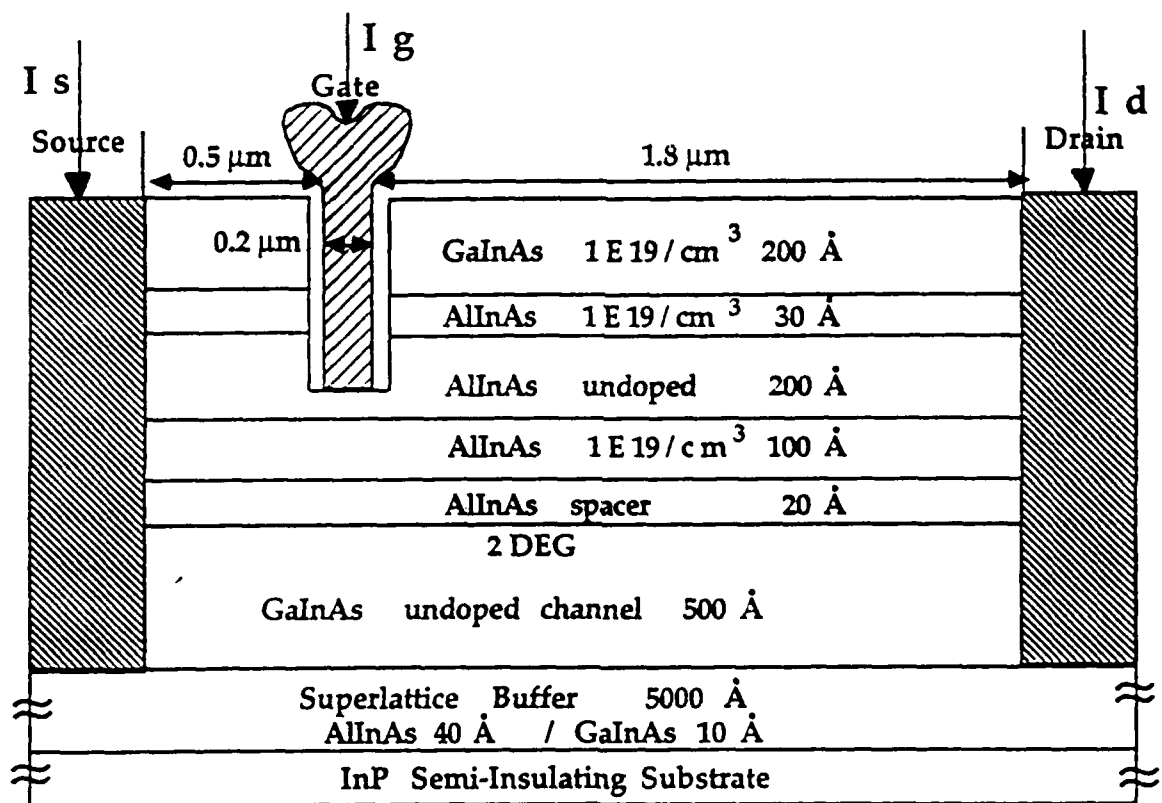
GATE LENGTH (μm)

Cross-sectional View of 0.2μm Gate Length AlInAs/GaInAs/InP MODFET
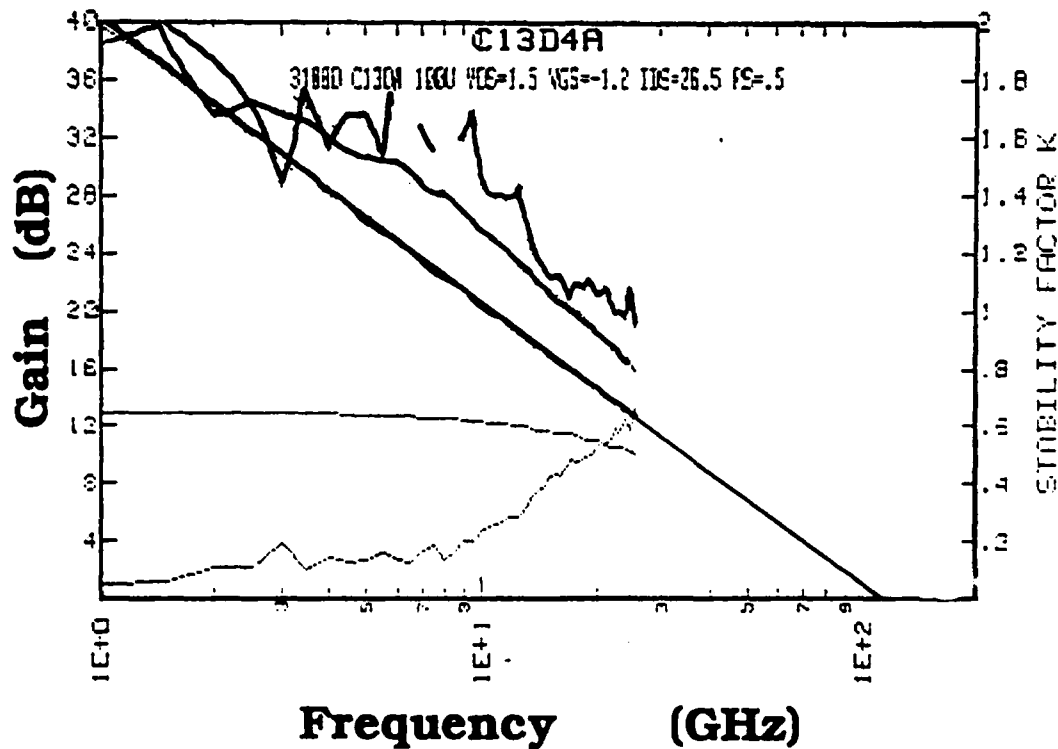
Current Gain and Power Gain Versus Frequency
0.2 μm T-Gate AlInAs/GaInAs/InP MODFET
AlInAs grown with low Arsenic over-pressure
f_T=110 GHz, f_{max}=220-250 GHz
V_d=1.5V, V_g=-1.2V, I_d=265mA/mm
100μm gate width, R_s=0.5Ω-mm
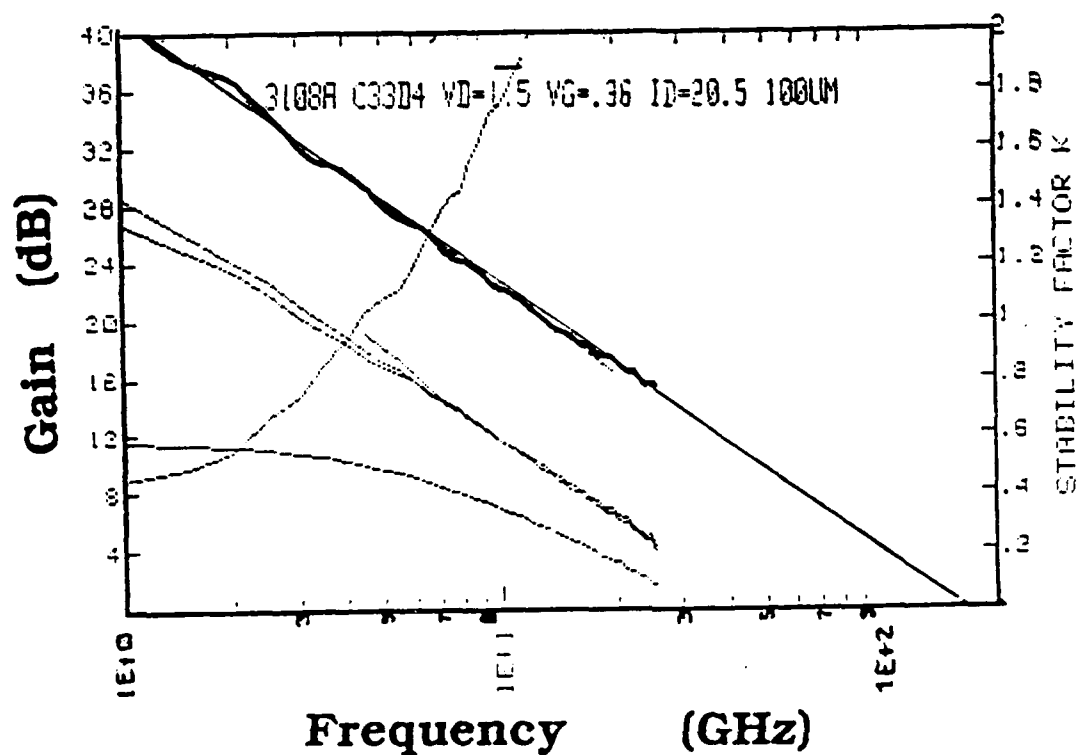
Current Gain Versus Frequency
0.1 μm Gate Length AlInAs/GaInAs/InP
MODFET
AlInAs grown with low Arsenic over-pressure
f_T=140-150 GHz
V_d=1.5V, V_g=+0.36V, I_d=205mA/mm
R_s=1.4Ω-mm, 100μm gate width

COMPOUND SEMICONDUCTOR STATE OF THE ART
2Q 1989 ON GaAs SUBSTRATES

MESFET

.1 μm M gate with AlGaAs buffer
600-700 mS/mm f_{tx} = 115 GHz

.25 μm gate with P GaAs buffer
Logic gate switching < 10 ps

MODFET

Doped $Al_3Ga_7As/GaAs$

.1 μm M gate, g_m - 450 mS/mm

f_{tx} = 113 GHz

.25 μm M gate 1.8 dB noise figure at 60 GHz

5^oK noise temperature at 8 GHz (12^oK)
.25 μm logic gates switching < 6 ps at 77K

SMODFET

Doped $Al_3Ga7As/In_yGa_{1-y}As/GaAs$

.10 μm M gate, y - .22, f_{max} = 345 GHz, f_{tx} = 60 GHz

.14 μm M gate, y = .25, f_{tx} = 153 GHz

I_{DS} = 500 mA/mm, f_{max} = 250 GHz

.25 μm M Gate, y = .22, 1W/mm, 50% power-added efficiency
.25 μm M gate, y = .15
1.6 dB noise figure at 60 GHz

20^oK noise temperature at 8 GHz (12^oK)

HBT

1.2 μm 5 x $10^{17}/cm^3$ emitter, 1 x $10^{20}/cm^3$ base
f_{tx} = 75 GHz, f_{max} = 175 GHz
Logic switching time 14 ps
f_{tx} = 105 GHz with ballistic electron collector

PBT

.25 μm period tungsten control electrodes in base
f_{tx} = 40 GHz, f_{max} = 265 GHz

COMPOUND SEMICONDUCTOR STATE OF THE ART
2Q 1989 ON InP SUBSTRATES

MISFET

1.0 μm gate with SiO_2 insulator

4.5 W/mm at 12 GHz, up to 45% efficiency

MODFET

Doped $Al_{.48}In_{.52}As/Ga_{.47}In_{.53}As/Al_{.48}In_{.52}As/InP$

.2 μm M gate - g_m = 800 mS/mm

f_{tx} = 125 GHz, f_{max} = 370 GHz

.8 dB noise figure at 60 GHz

Logic gate switching 6.0 PS @ 300 K, 4.8 Ps @ 77K

.15μm M gate - g_m = 1320 mS/mm, f_{tx} = 186 GHz (50 μm)

SMODFET

Doped $Al_{.48}In_{.52}As/Ga_{.35}In_{.65}As/Ga_{.47}In_{.53}As/InP$

.10 μm M gate, f_{tx} = 210 GHz (200 μm)

HBT

$InP/In_{.53}Ga_{.47}As/InP$ - 3.6 x 3.6 μm

Emitter doped to $.5-1x10^{18}/cm^3$, base to $5x10^{20}/cm^3$

f_{tx} = 165 GHz, f_{max} - 100 GHz @ 300K

f_{tx} = 244 GHz at77K

COMPOUND SEMICONDUCTOR TRANSISTOR
PREDICTED PERFORMANCE

SMODFET - Al,GaAs/In,GaAs/Al,GaAs/GaAs

.1 μm M gate and p doped buffer

1000 mS/mm, .8 A/mm

f_T = 200 GHz, f_{max} = 400 GHz

Switching time < 4 PS

MODFET - Al,InAs/GaInAs/AlInAs/InP

.1 μm M gate and P doped buffer

1200 mS/mm, > 1A/mm

f_T = 250 GHz, f_{max} = 500 GHz

HBT - Al,GaAs/In$_y$Ga$_{1-y}$As/GaAs

Submicron emitter, fast electron transit,

1-5 x 10^5A/cm^2

f_T = 200 GHz, f_{max} = 400 GHz

Switching time < 4 Psec.

InP/In$_{.53}$Ga$_{.47}$As/InP

Submicron emitter, near ballistic electrons

2-5 x 10^5A/cm^2, switching time 2PS

f_T = 400 GHz, f_{max} = 500 GHz

PBT - GaAs with Tungsten Control Electrodes

f_T = 100 GHz, f_{max} = 400 GHz

High operating voltage for power

GAIN AND NOISE CHARACTERISTICS OF InAlAs/InGaAs STRAINED HEMTS

Dimitris Pavlidis, Geok Ing Ng and Matthias Weiss

Center for High Frequency Microelectronics
Solid State Electronics Laboratory
Department of Electrical Engineering and Computer Science
The University of Michigan
Ann Arbor, MI 48109-2122

InP Based Microwave/Millimeter Wave Technology Workshop

San Diego, Ca

January 25 - 26, 1989

Gain and Noise Characteristics of InAlAs/InGaAs Strained HEMT's

Dimitris Pavlidis
Geok Ing Ng
Matthias Weiss

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OUTLINE

- STRAINED LAYER DEVICE PRINCIPLES AND DESIGN

- MOBILITY AND VELOCITY CHARACTERISTICS

- DC. AND LOW FREQUENCY PROPERTIES

- MICROWAVE PERFORMANCE AND GAIN

- LOW - FREQUENCY NOISE

- DOUBLE HETEROJUNCTION DESIGN AND MICROWAVE
  PERFORMANCE

- CONCLUSIONS

Cross - Section of InGaAs/InAlAs HEMT

Ohmic Contacts (Ge/Au/Ni/Ti/Au)

Schottky Contact (Ti/Au)

Strained Channel (x=0.60, 0.65)
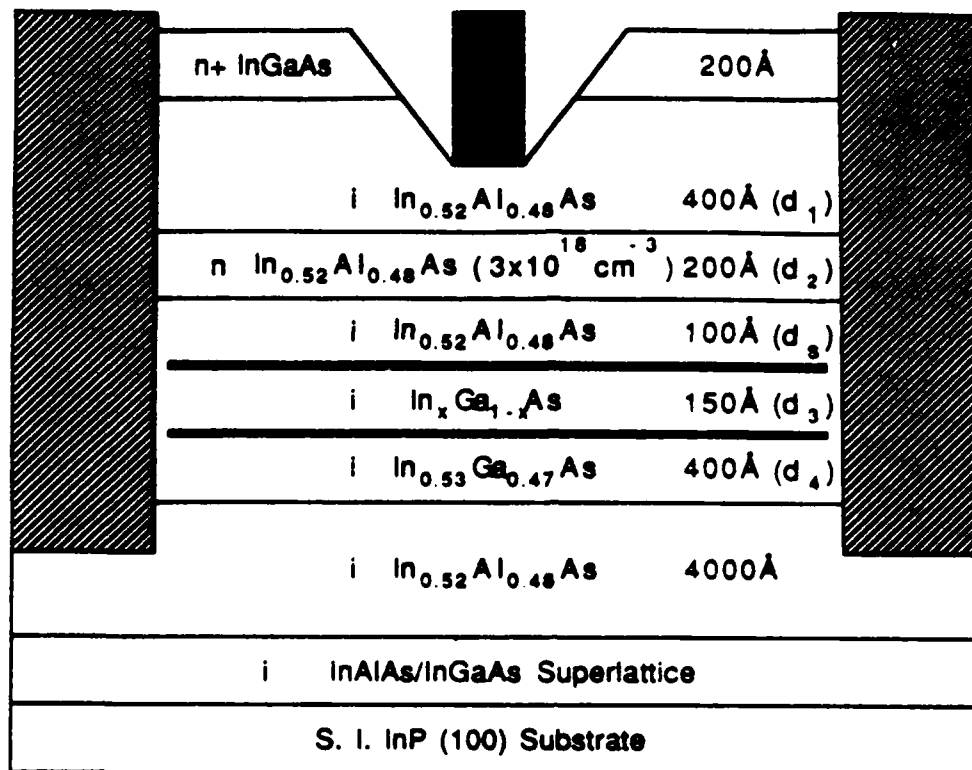
* Strain introduced for $x > 0.53$ in the channel

* Si doping efficiency of AlInAs can be very high

$$(N_d ==> > 10^{19} cm^{-3}) ==> N_s \; \hat{\|}$$

but

* Gate Leakage ==> i - InAlAs

* InGaAs Background conductivity control

Strained (-) vs Lattice Matched (--) InGaAs/InAlAs HEMT's

* $E_1 - E_0$ increases and E_0 occupation is higher
  (1.12×10^{12} to 1.65×10^{12} cm^{-2} for X : 0.53 to 0.65)

* ==> reduced scattering ==> $\mu \uparrow$

* $\Delta E_C \uparrow$

* m^* (strained) $\downarrow$

Larger improvement for Strain-Relief Channel Designs
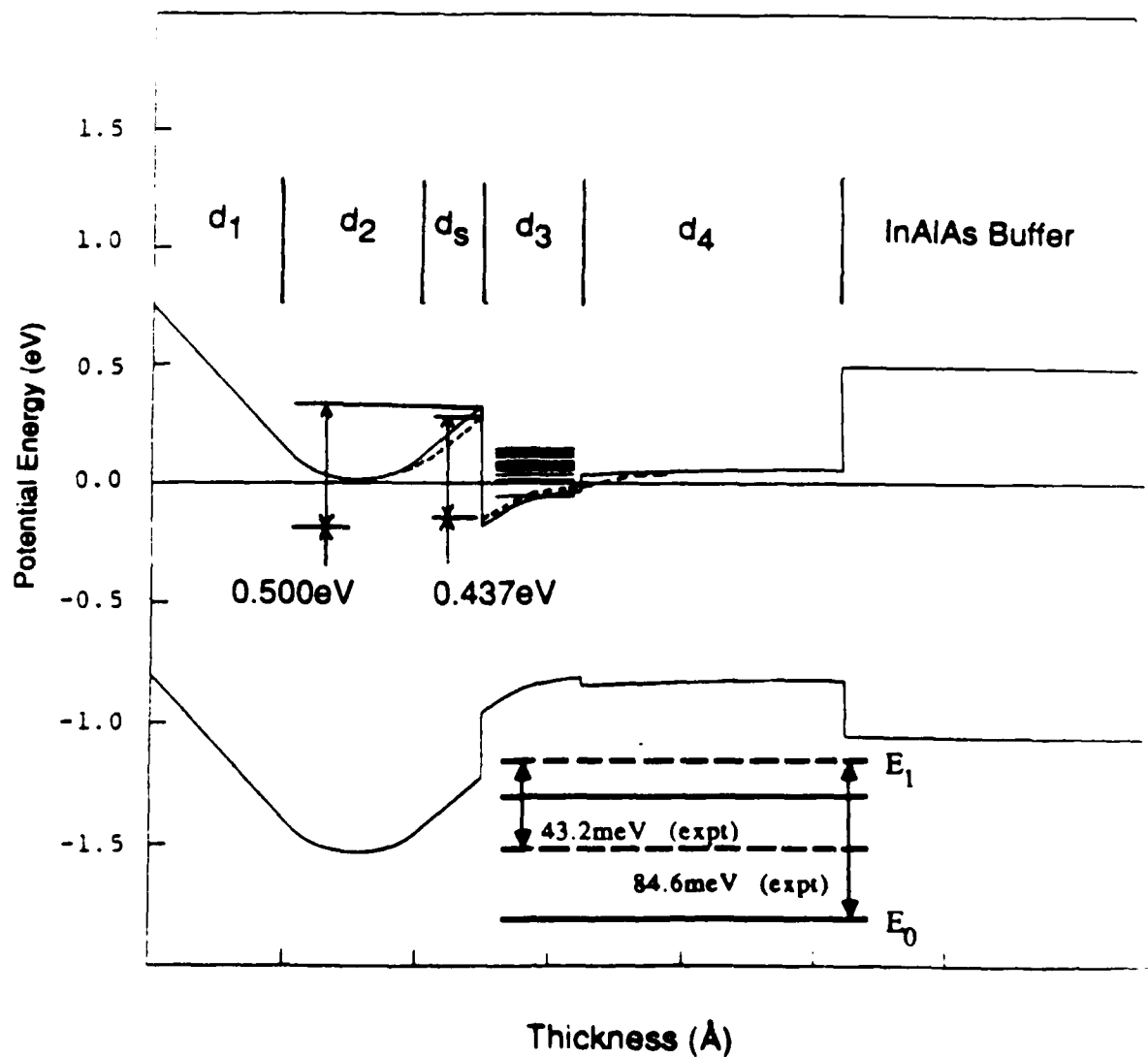
Effect of Strained Designs on $\mu ==> T$ and N_s vs T Characteristics

* $\mu \stackrel{\wedge}{\|}$ with In-percentage

*   Best performance for optimum (150Å channel) design

*   At low T : reduced Alloy Scattering with $X \stackrel{\wedge}{\|}$

*   At high T : combined Alloy + Polar Phonon Scattering

    (Alloy Scattering reduced with $X \stackrel{\wedge}{\|}$)
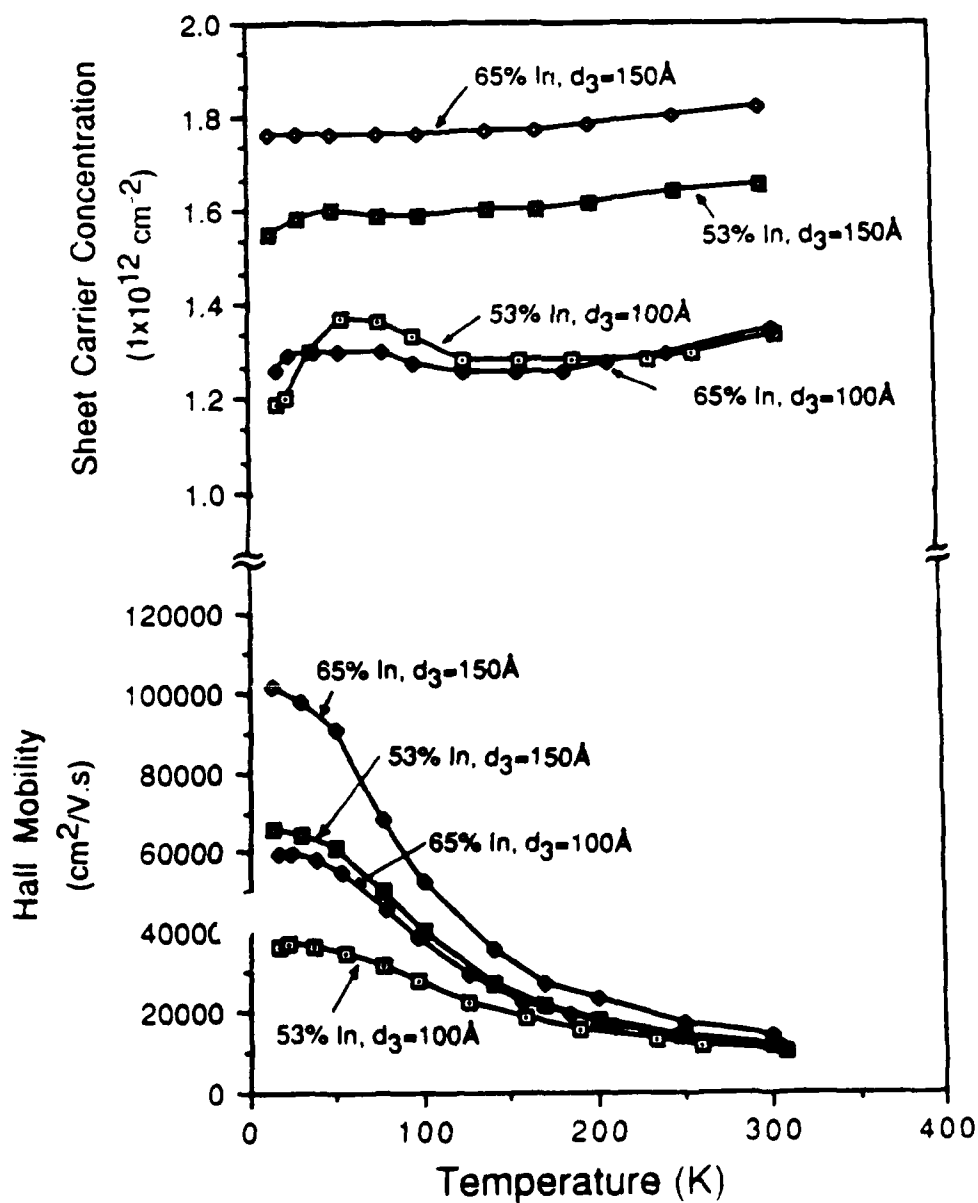
Experimental Velocity-Field Characteristics of Strained Heterostructures N-Channel: InGaAs/InAlAs with 12% Excess Indium

Improved Transport by :   * High InAs mole fraction

* Large E_1 - E_0 separation and reduced scattering

* Better Confinement

@ 2.25kV/cm

53%-In   V= 1.35×10^7 cm/sec ----------
60%-In   V= 1.45×10^7 cm/sec +7.4% ΔV improvement
65%-In   V= 1.55×10^7 cm/sec +14.8% ΔV improvement
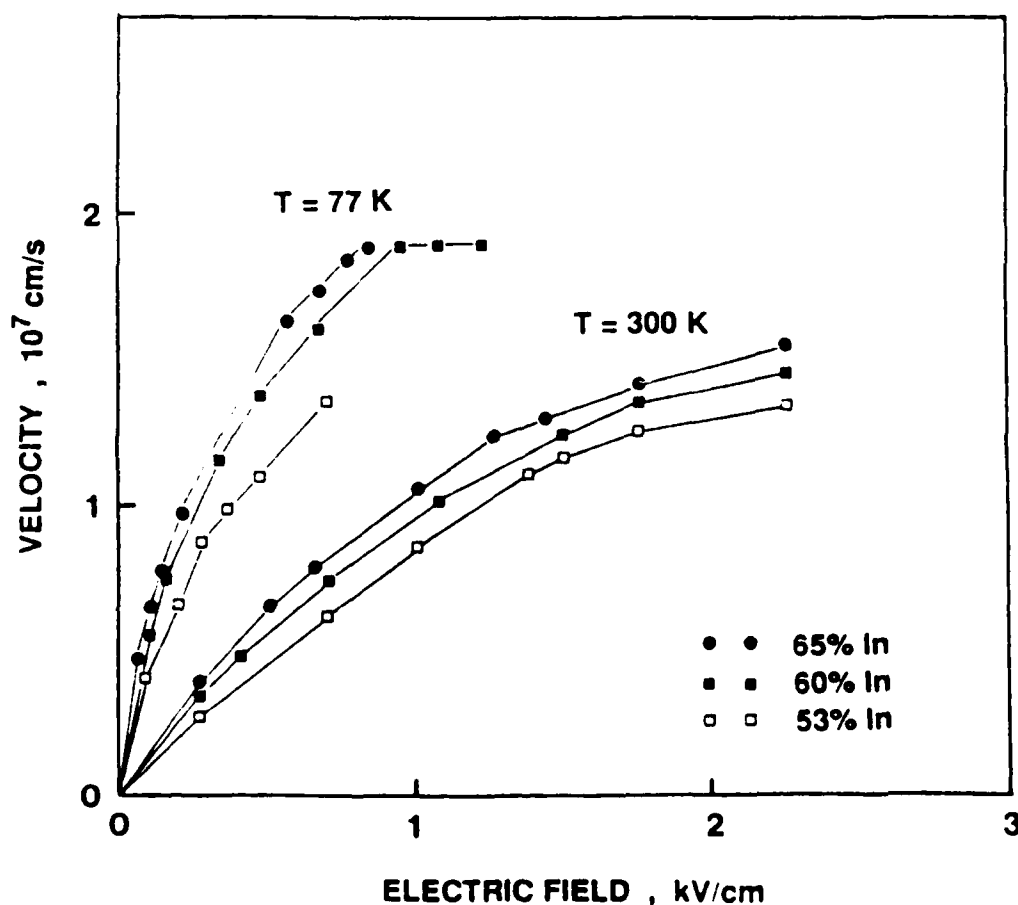
I_{ds}-V_{ds}, G_m-V_{gs} and I_{dss}-V_{gs} Characteristics of Strained (65% In) InGaAs/InAlAs HEMT (d_3 = 150Å, L_g = 1µm)
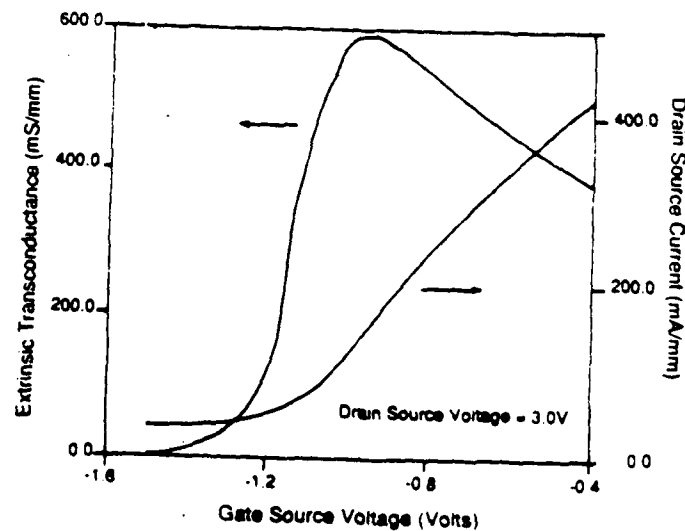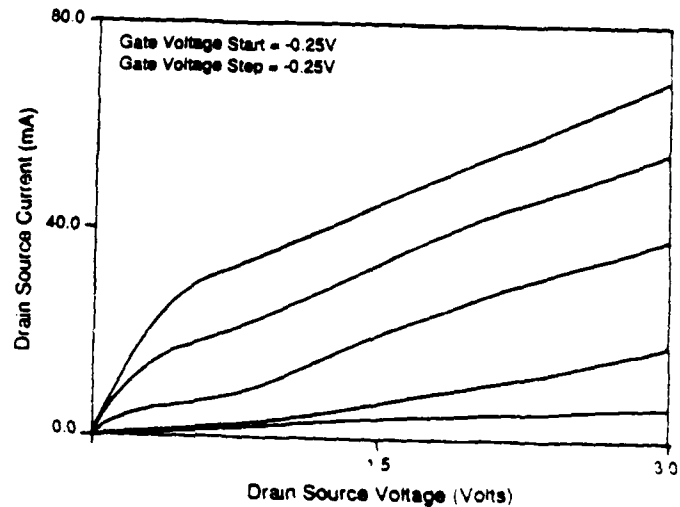
I_{dss} (V_{gs} = OV, V_{ds} = 3V)   = 550 mA/mm

G_{mmax} (V_{gs} = -0.975 V, V_{ds} = 3 V)   = 830 mS/mm - Intrinsic

                                            = 590 mS/mm - Extrinsic

G_{ds} = 39mS/mm (Compare to 33mS/mm with 53% In)

Transcendance Histograms for 60% and 65% Indium InGaAs/InAlAs HEMT's
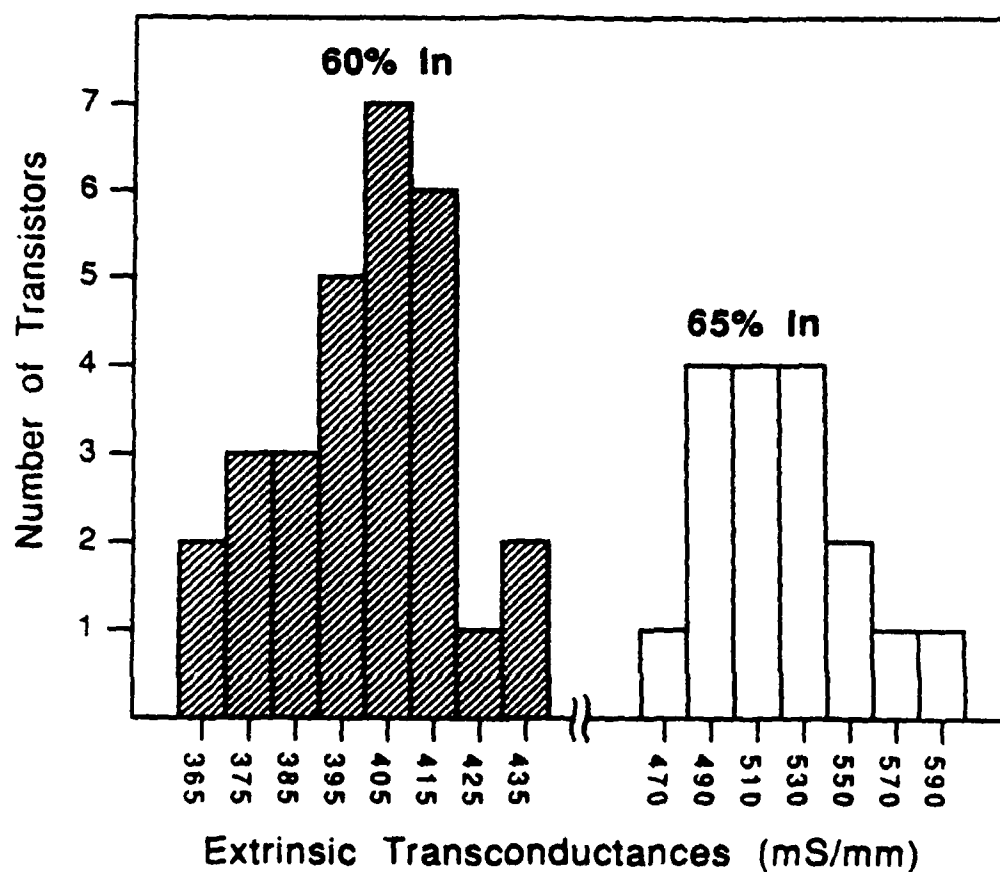
	$\bar{g}_{mextrinsic}$ (mS/mm)	$\bar{g}_{mintrinsic}$ (mS/mm)
X = 0.60	400	500
X = 0.65	520	700
V_{th} (0.2σ)	-1.13 ± 0.048	-1.11 ± 0.046

overall g_m improvement with X $\overset{\wedge}{\underset{=}{}}$

Bias Dependence of Microwave Output Resistance

* $R_{ds} \Downarrow$ for $x \Uparrow$ ==> μwave tendency is similar to DC

* $R_{ds} \Downarrow$ for $x = 0.65$ and large V_{ds}, $|Vgs|$ => carrier &

Substrate injection
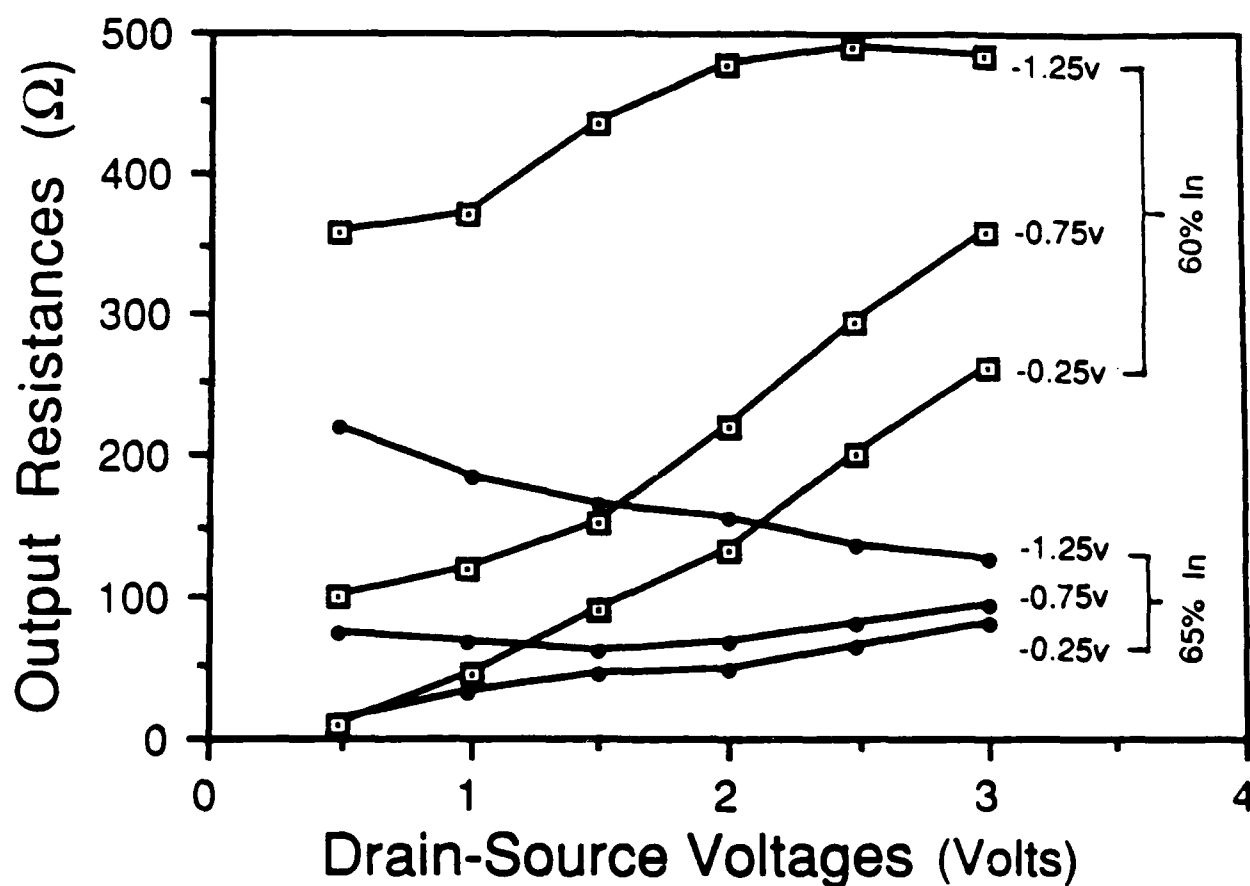
	60%	65%
$(g_m/g_d)_{DC}$	11	6
$(g_m/g_d)_{RF}$	14	5

Power Gain, Cutoff and Maximum Oscillation Frequency

1 μm X 150 μm InGaAs/InAlAs HEMT's

60%
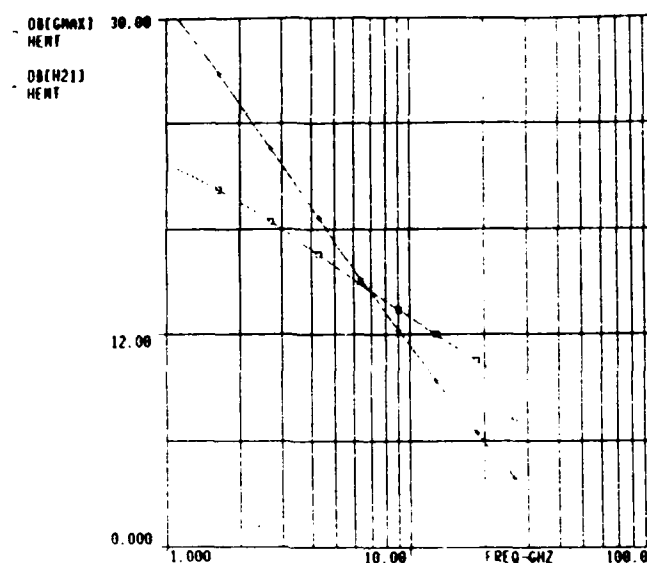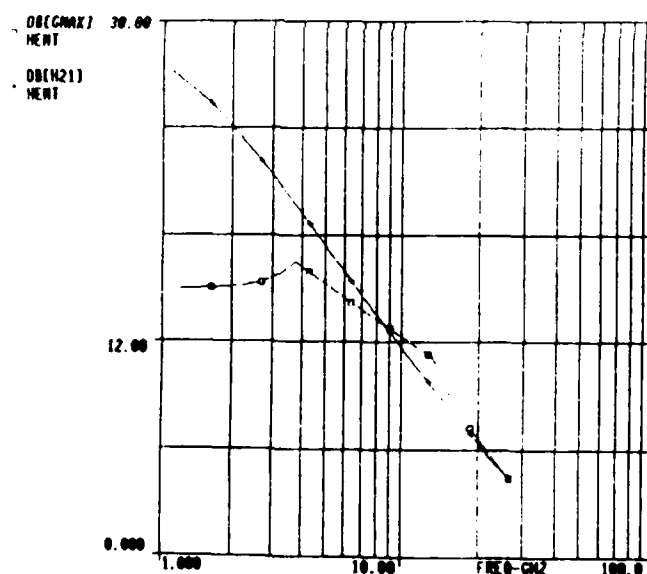
ω5%

	f_t	Power G (10GHz)	Power G (18GHz)	f_{max}
X = 0.60	40GHz	13dB (MSG)	10.6dB (MSG)	60GHz
X = 0.65	45GHz	12.3dB (MSG)	7.5dB (MAG)	46GHz

Low- Frequency Output Resistance Characteristics
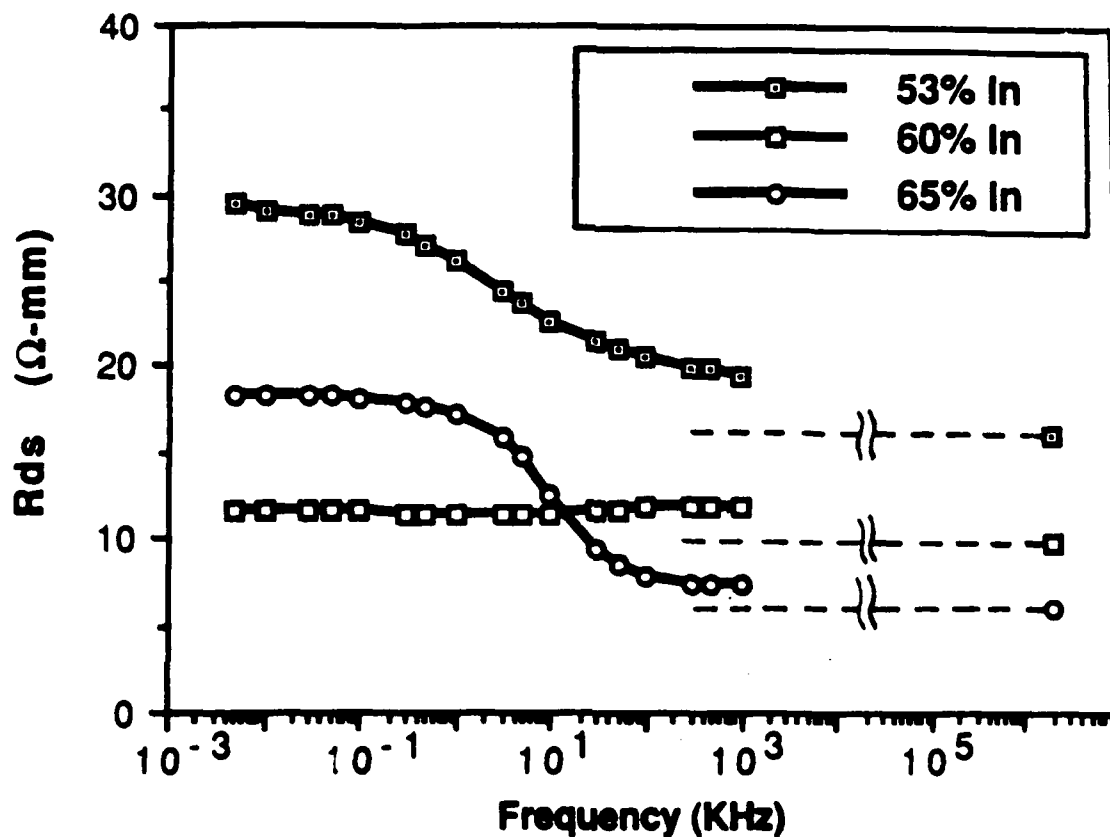
$R_{ds} \hat{\parallel}$ at low frequencies (interface states responding to AC-signal)

* Minimum R_{ds} dispersion for $x \approx 0.60$

==> Better interface quality for small In-content

Low-Frequency Noise Characteristics

* Voltage Noise Source Spectrum Density (S_V) at device input
* Bias conditions for minimum noise correspond approximately to g_{max} condition

* $1/f^n$: n = 1 signifies 1/f noise
    n = 1.5 signifies transmission-line thermal noise
    n = 2 signifies g-r noise

	n (f= 610MHz)	SV(V^2Hz)	V_{gs}(V)	V_{ds}(V)
53%	0.57	3.2×10^{-17}	-1.37	3
60%	0.61	5.0×10^{-17}	-0.523	3
65%	0.81	2.0×10^{-17}	-0.464	2
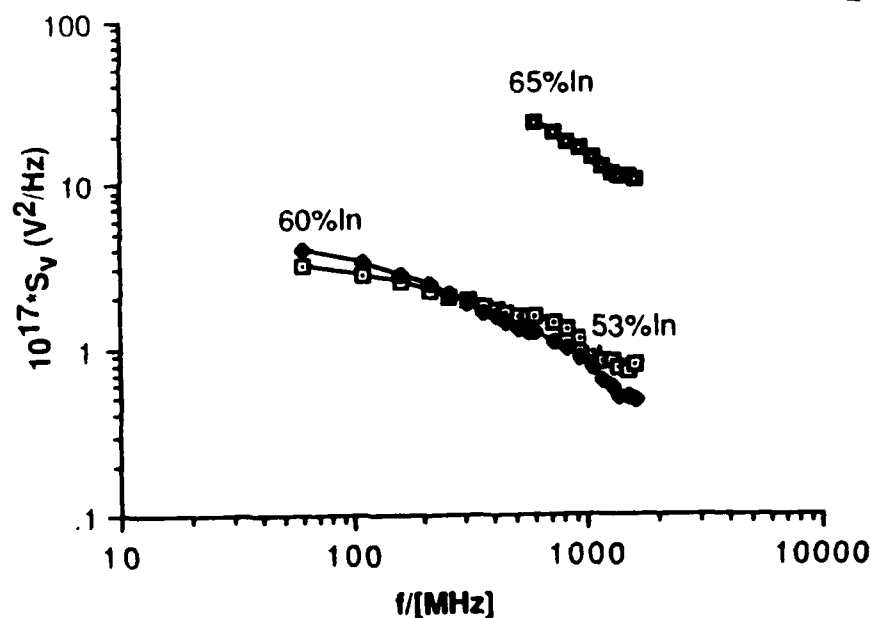
* Small In-composition increases do not influence appreciably the noise level

* High Corner Frequencies increasing with In compensation

* Consequences on analog circuits and oscillators

Improving Microwave Characteristics With Double Heterojunction Designs
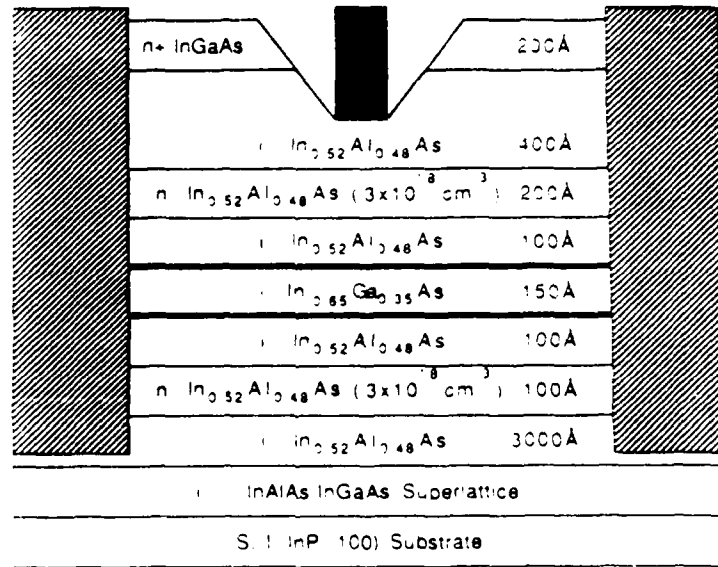
Device Cross-Section

* Thinner bottom layer ==> no parasitic conduction

* Design Basics

	%center in QW	E_0 Occupancy	% carriers in top (Donor + Spacer)	% Carrier in bottom or L.M. layer
Single heterojunction	78.3	85.7	11.5	10.3
Double heterojunction	85.7	74	6	7.3

==> Strained QW occupation larger in DH-HEMT design

==> Better carrier confinement

* No double-humped E_0 - wavefunction for 150Å design

Mobility (μ), Sheet-Carrier (n_s) Data
(150Å Channel, 65% In)

Growth Interruption Time (sec)		μ (cm^2/V$_s$)	n_s (x 10^{12} cm^{-2})
30	T = 300 K	10,700	2.32
	T = 77 K	29,500	2.27
120	T = 300 K	4,650	2.41
	T = 77 K	27,550	2.28

* Inverted heterointerface limits overall mobility

* Best characteristics by growth interruption optimization

DC - Characteristics of 65% -In DH - HEMT (Lg = 1µm)
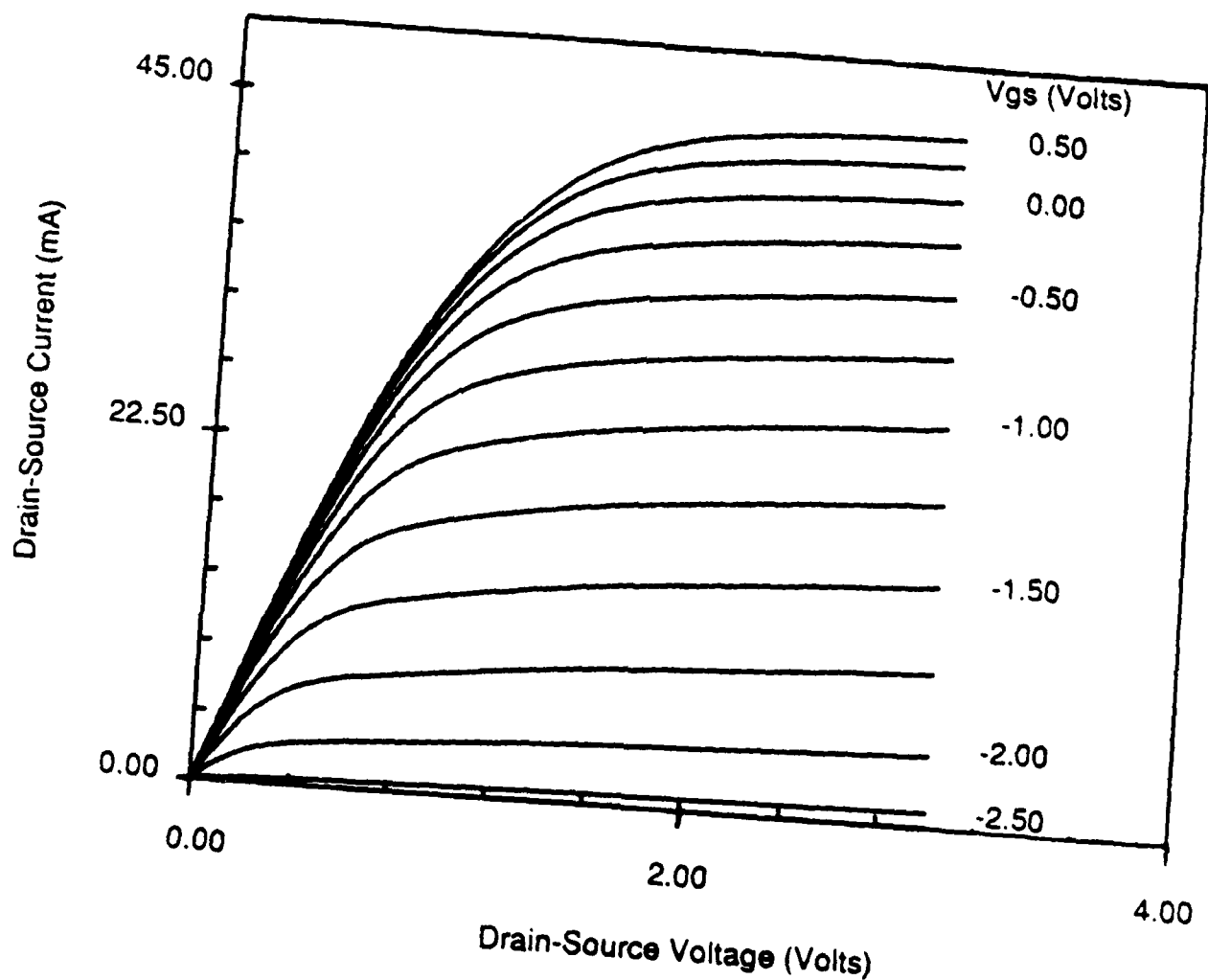
* $G_{ds} = 13 mS/mm$

* Reduction of G_{ds} by a factor of 3 compared to single-heterojunction lattice-matched or strained designs

* $I_{dss} = 540\ mA/mm$ @ $V_{gs} = 0V,$ $V_{ds} = 3V$
  $I_{dss} = 600\ mA/mm$ @ $V_{gs} = 0.5V,$ $V_{ds} = 3V$

Transfer Characteristics of 65% -In DH-HEMT (L_g - 1um)
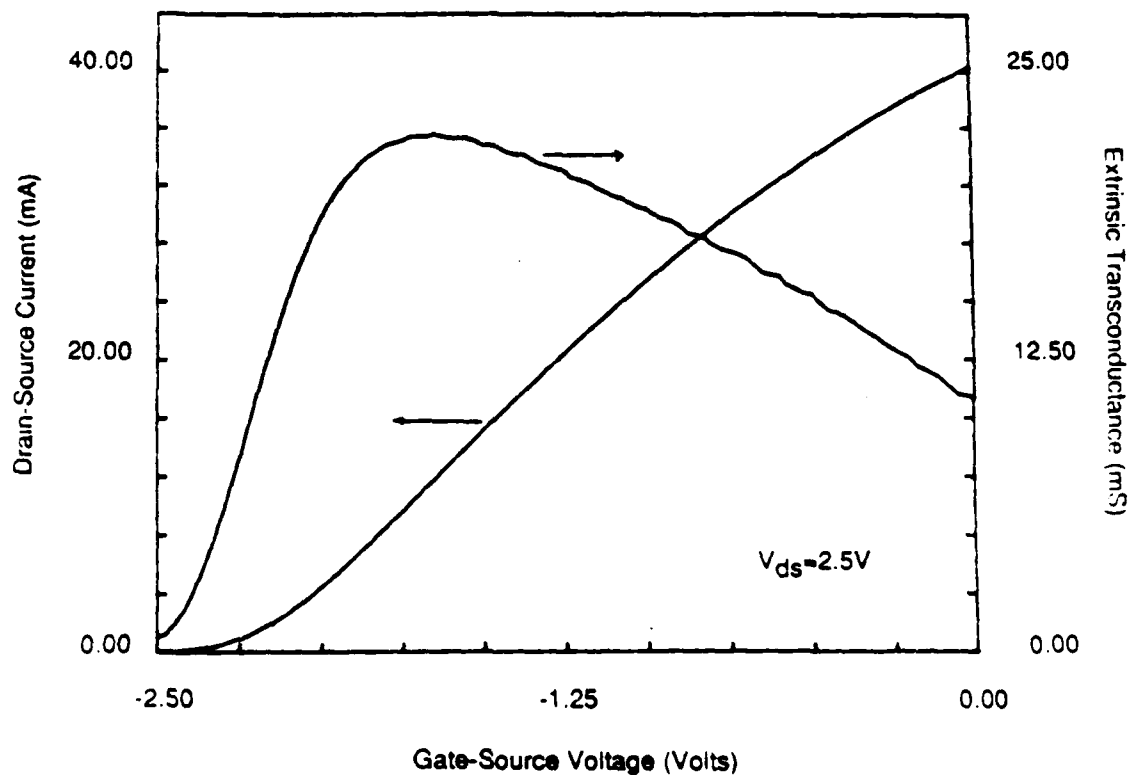
* g_{mextr} (Max) = 296 mS/mm @ V_{ds} = 2.5V, V_{gs} = -1.4V

* g_{mint} (Max) = 532mS/mm

ie. lower than for single HEMTs :   — smaller E_o occupation

— larger wavefunction spread

* I_{dss} @g_{mextr} (max) = 140mA/mm

  I_{dss} is larger than for single HEMT's of equivalent doping

  (~ 100 mA/mm)

* Small g_m - V_g dependence

  ==> better intermodulation distortion

* g_m/g_d = 22

Power Gain, Cutoff and Maximum Oscillation Frequency

1μm x 75μm InAlAs/InGaAs HEMT
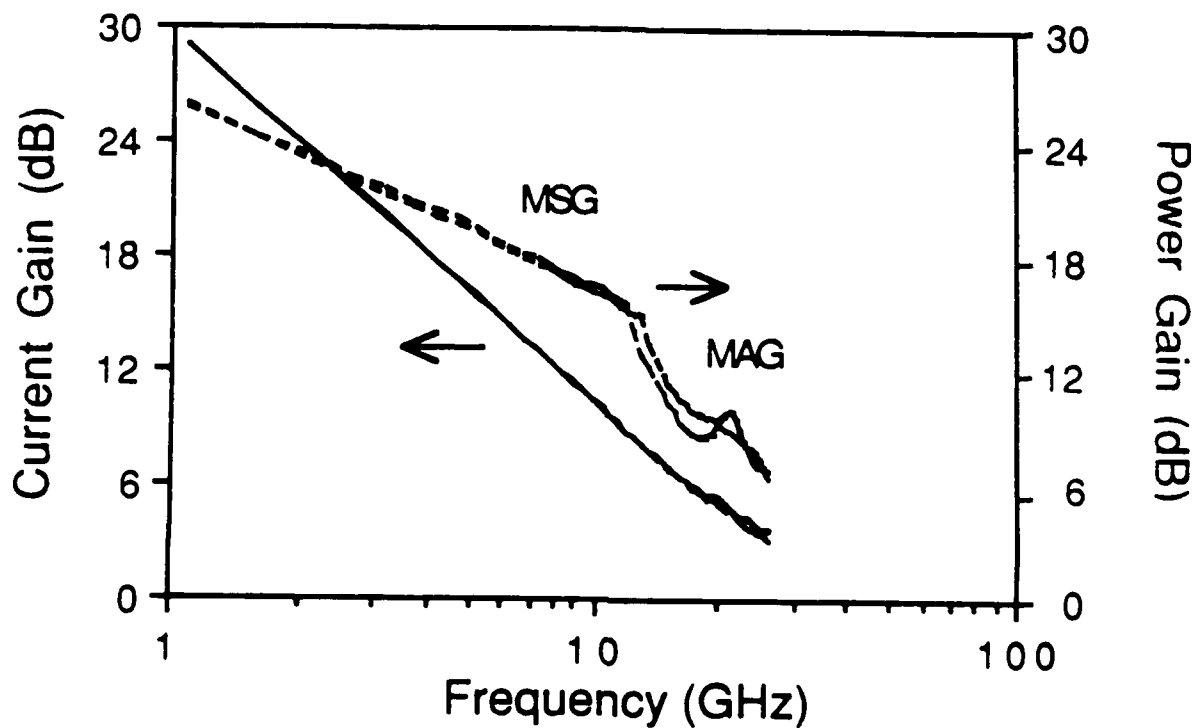
* $f_T \approx 37$ GHz

* $f_{max} \approx 66$ GHz

*   Unconditional Stability (k > 1)   @ f > 13 GHz

*   9.6 dB MAG @ 20 GHz

Conclusions

- The DC, Low-Frequency and Microwave Characteristics of Strained N-Channel HEMT's have been investigated.

- The mobility, velocity and transconductance, as well as, cutoff frequency improve with In-composition.

- The output conductance decreases with In composition.

- The low-frequency noise characteristics degrade with very high In- content.

- The Maximum-Oscillation frequency and Power gain of strained-HEMT's improve with double-heterojunction design.

NON-STATIONARY TRANSPORT PHENOMENA IN INDIUM PHOSPHIDE-BASED
HETEROJUNCTION BIPOLAR TRANSISTORS

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Non-Stationary Transport Phenomena in Indium Phosphide-based Heterojunction Bipolar Transistors*

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Basic equations

Static behavior :

current gain in common base configuration

$$a = \gamma \ B \ M$$

$$M \approx 1$$

$$B = 1 - \frac{t_b}{\tau_n} \qquad \text{Transport ratio}$$

$$\gamma = \frac{J_n}{J_n + J_p} \approx 1 - \frac{J_p}{J_n} \qquad \text{Injection ratio}$$

Dynamical behavior :

Cutoff frequency

$$f_t = \frac{1}{2 \pi \ t_t} \quad \text{with} \qquad t_t = \tau_{BE} + t_B + t_C + \tau_{BC}$$

Maximum oscillation frequency

$$f_{max} = \sqrt{\frac{f_t}{2 \pi \ R_B \ C_C}}$$

with R_B : base resistance
C_C : base-collector capacitance

Selective Injection through Heterojunction
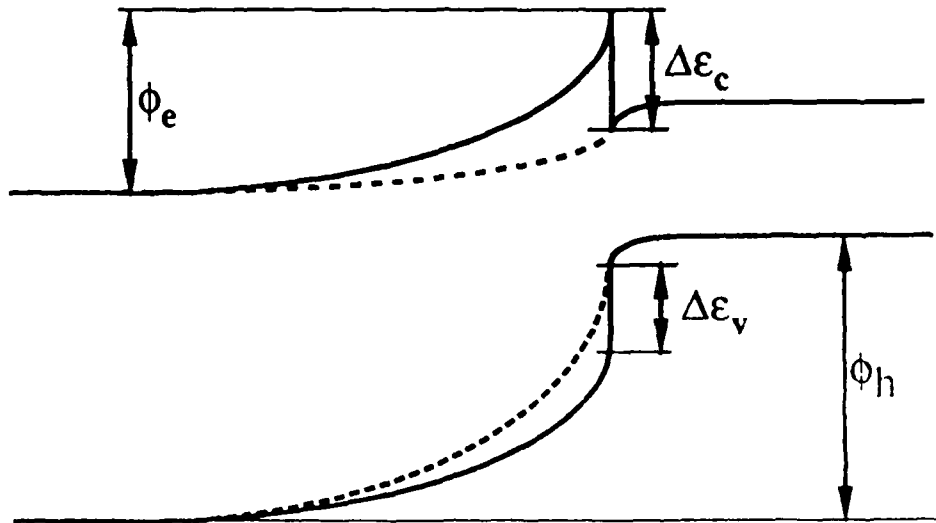
$$\left(\frac{Jp}{Jn}\right)_{hetero} \approx \left(\frac{Jp}{Jn}\right)_{homo} \exp\left(\frac{\phi_e - \phi_h}{kT}\right)$$
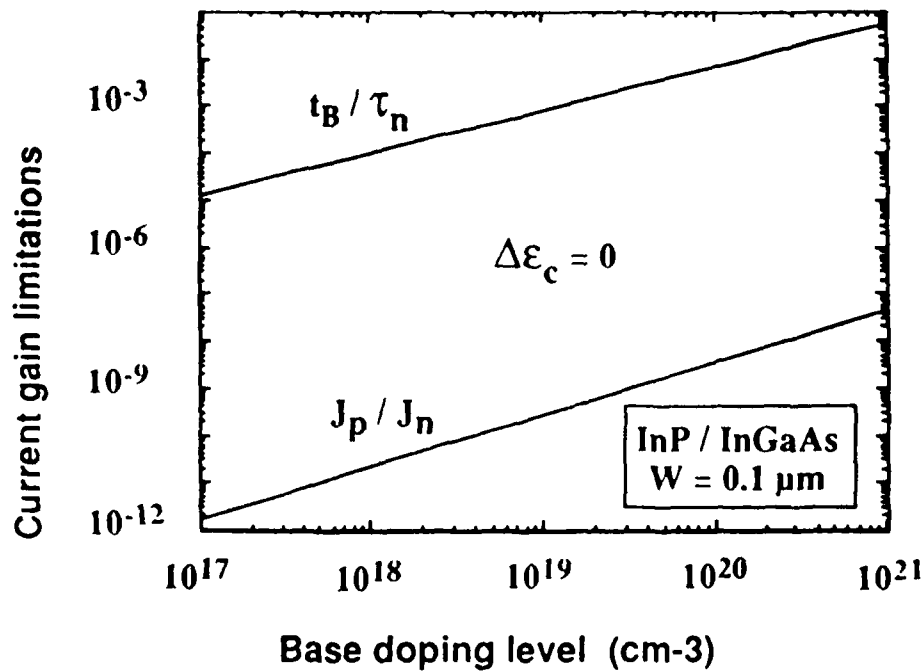
Ballistic and quasi-ballistic transport
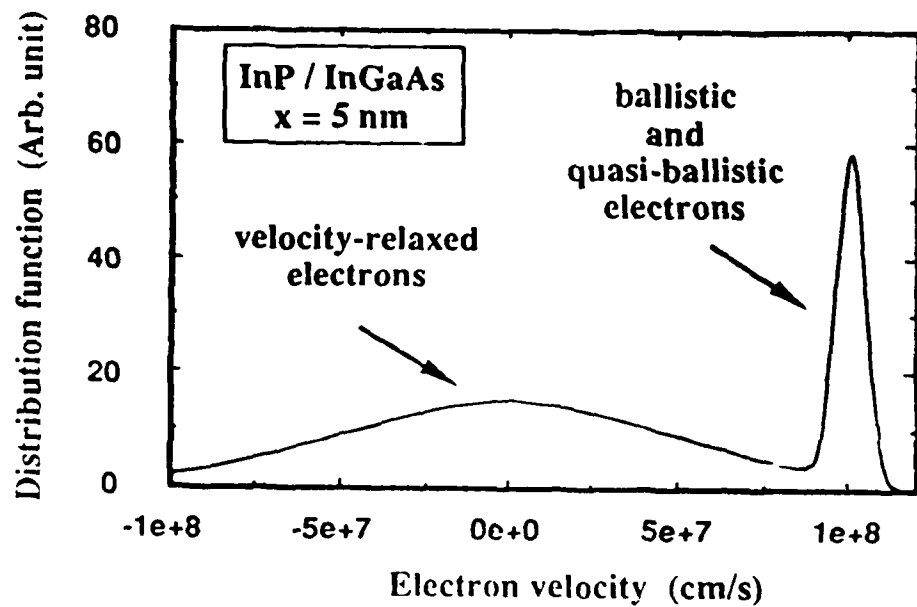
$$J_{QB}(x) = J_{QB}(0) \exp\left(\frac{-x}{\Lambda}\right) \quad \text{with } \Lambda = \frac{v_{QB}}{\lambda_{total} - \lambda_{non-iso}}$$

$$B = 1 - \frac{W_B^2}{2L_n^2} f$$
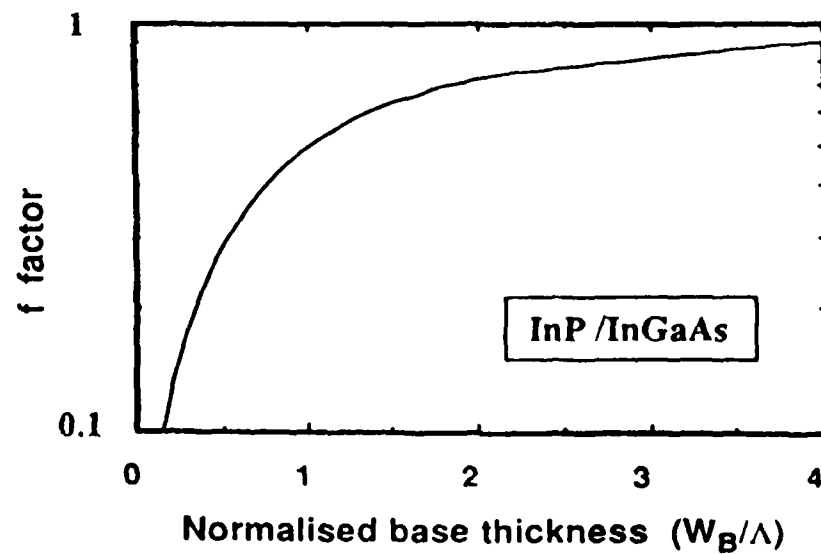
Transport factor
limitation

Injection factor
limitation

$N_A = 1 \times 10^{19}$ cm^{-3}

$N_A = 5 \times 10^{19}$ cm^{-3}

$N_A = 3 \times 10^{20}$ cm^{-3}

InP/InGaAs
W = 0.1 µm

Current gain

Conduction band discontinuity (eV)

$N_A = 8 \times 10^{18}$ cm^{-3}

$N_A = 2 \times 10^{19}$ cm^{-3}

$N_A = 4 \times 10^{19}$ cm^{-3}

$N_A = 8 \times 10^{19}$ cm^{-3}

AlGaAs/GaAs
W = 0.1 µm

Current gain

Conduction band discontinuity (eV)
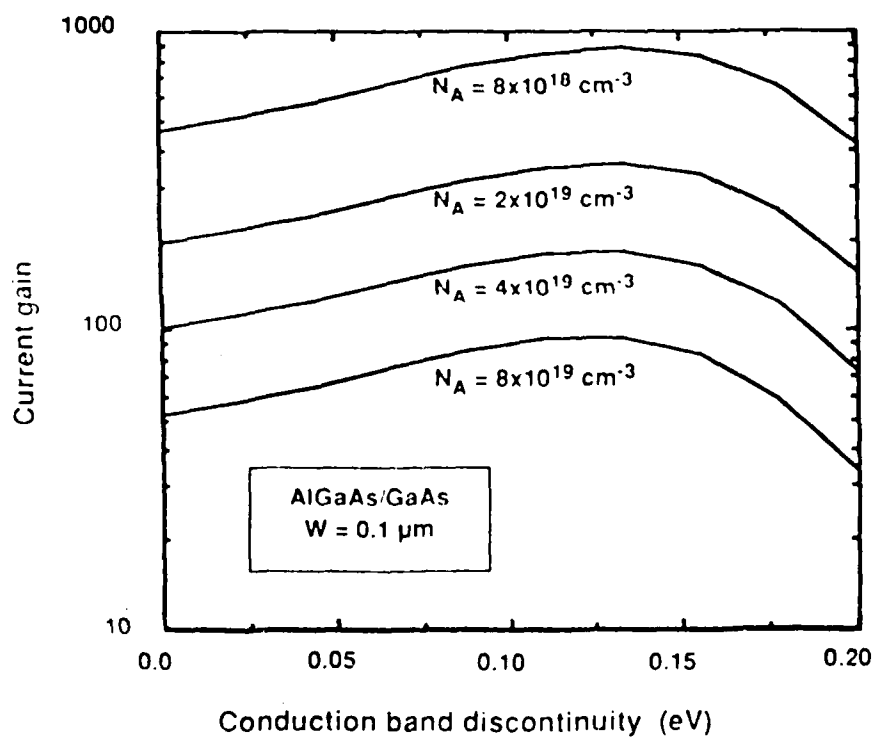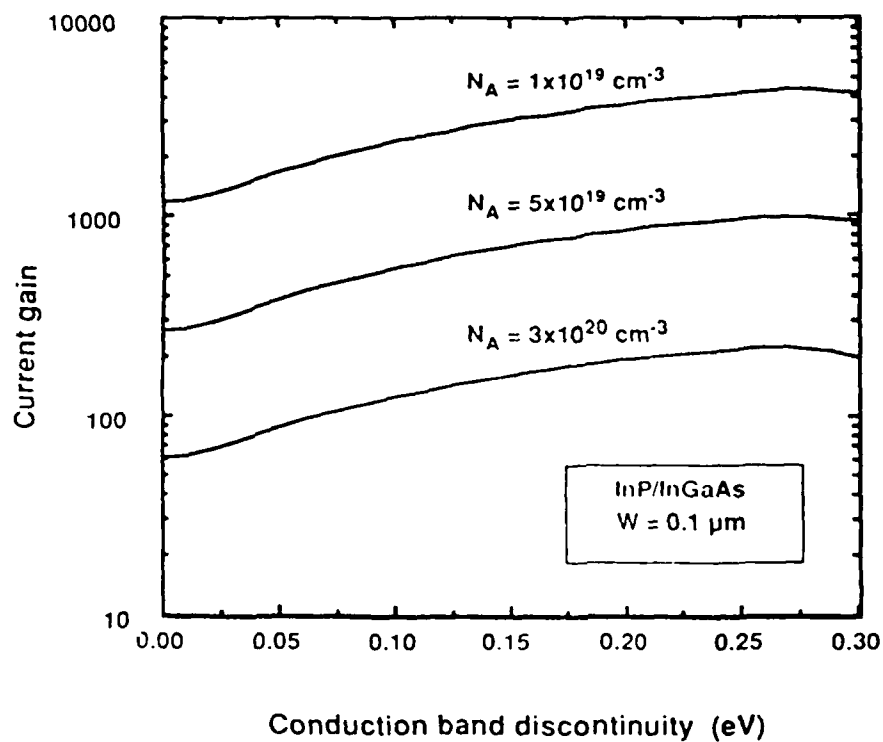
Conclusions

* There exists an optimum value of the conduction band discontinuity in the emitter-base hetero-junction leading to a maximum value of the current gain.

* This effect can be used to improve

    . the static behavior
  or
    . the dynamical behavior at a given current gain

* This effect is easier to use in the InP-based system than in the GaAs-based system:

    . optimum value close to the value of the abrupt junction

    . larger effect (x5 instead of x2)

    . smaller recombination velocity at the interface (MOMBE)

ANALYTICAL AND COMPUTER-AIDED MODELS OF InP-BASED MISFETS* AND
HETEROJUNCTION DEVICES**

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University of California
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♦♦Naval Ocean Systems Center
San Diego, CA

Analytical and Computer-Aided Models of

InP-Based MISFETs[*] and Heterojunction Devices[**]

A. J. Shey[+], W. H. Ku[+], and L. Messick[++]

[+] Dept. of Electrical and Computer Engineering, University of California, San Diego

[++] Naval Ocean Systems Center, San Diego

- Introduction

- 1-D MISFET Model *

- 2-D HEMT Model **

- Summary

Typical Distribution of Interface State Density within Energy Band Gap

Measured by C – V or Optical Methods

From P. D. Gardner et al. IEEE Electron. Dev. Lett.,

EDL-8 (1987) 45.

From H. H. Wieder, Surface Science 133 (1983) 390.

Typical Distribution of Interface State Density within Energy Band Gap Measured by C – V or Optical Methods
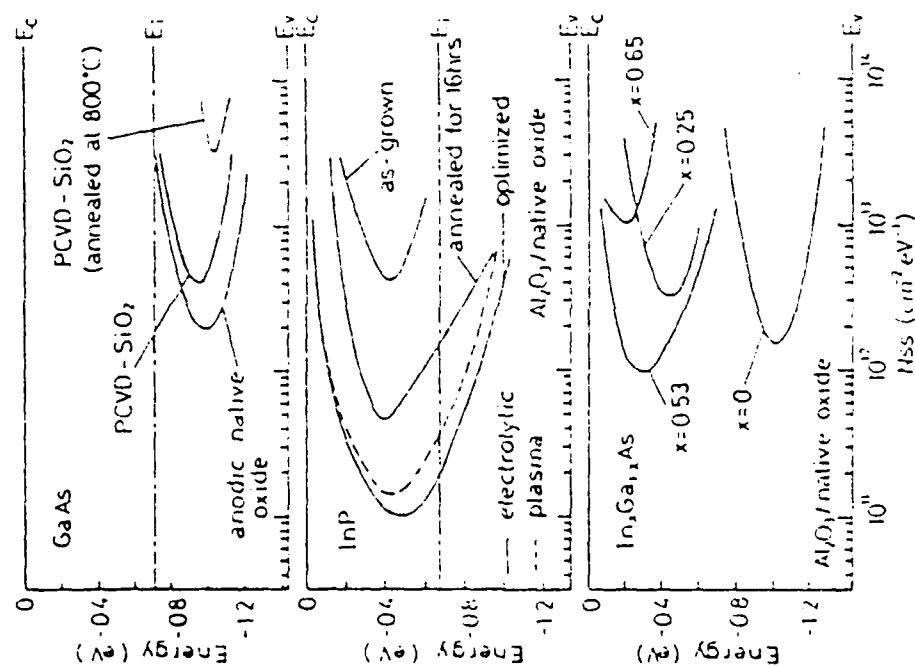
Measured N_{ss} distribution of the I-S interfaces, using C-V and PCTS methods. Note that no peaks in the N_{ss} distribution are observed. While minimum N_{ss} and U-shape curvature depends on processing conditions, the location of N_{ss} minimum remains constant for each semiconductor.

From H. Hasegawa et al. *J. Vac. Sci. Technol.*, B, Vol. 4, (1986) 1130.

Energy band diagram of an n-type InP MIS structure

Equilibrium Condition

Gate Bias Applied
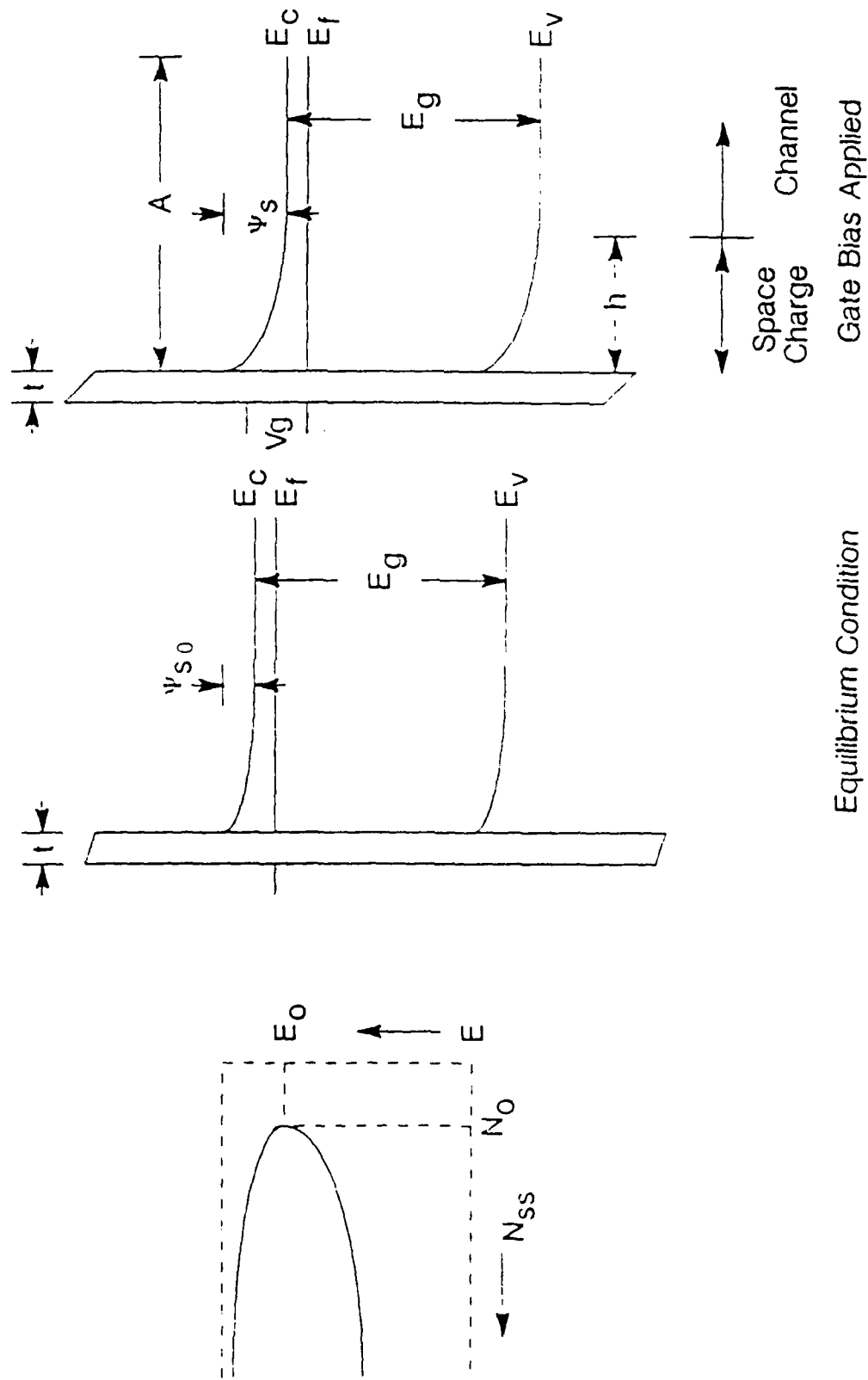
Charge control model

By Gauss law

Electrical field at the interface of insulator and semiconductor

$$E - E_o = -\frac{1}{\epsilon_d}\left[(Q_s - Q_{so}) + (Q_{ss} - Q_{sso})\right]$$

Q_s : space charge

Q_{ss} : interface state charge

subscript o : equilibrium state value

$$V_g - V(x) = -\frac{t}{\epsilon_d}\left[(Q_s - Q_{so}) + (Q_{ss} - Q_{sso})\right] + (\psi_{so} - \psi_s)$$

t : insulator thickness

ϵ_d : insulator permittivity

V(x) : channel potential

ψ_s : surface potential

Distribution of interface states within energy band gap

Existing model (uniform interface states distribution model)[*] :

$$N_{ss} = N_o \quad : \quad constant$$

$$\Delta Q_{ss} = q N_o (\ \psi_s - \psi_{so}\ )$$

Hasegawa's DIGS model :

$$N_{ss} = \begin{cases} N_o\, exp\left[\left(\dfrac{E - E_o}{E_{oa}}\right)^{n_a}\right] & E \geq E_o \\[2ex] N_o\, exp\left[\left(\dfrac{E_o - E}{E_{ob}}\right)^{n_b}\right] & E \leq E_o \end{cases}$$

$$\Delta Q_{ss} = -q \left[\int N_{ss}\, f(E)\, dE \Big|_{\psi_s} - \int N_{ss}\, f(E)\, dE \Big|_{\psi_{so}} \right]$$

$f(E)$: the occupation function

Variable interface states distribution model :

Simplified Hasegawa's model with $\quad n_a = n_b = 1.0$

[*] R. Pucel et al., Advances in Electronics and electron Devices, 38 (1975) 195.

D. Lile, Solid-State Electron., 21 (1978) 1199.

P. Hill, IEEE Trans. Electron Devices ED-32 (1985) 2249.

The empirical velocity versus electrical field model [*]

$$
\upsilon = \begin{cases} \dfrac{\left(\mu + \dfrac{\upsilon_{sat}}{E_C}\right) E}{1 + \dfrac{E}{E_C}} & E \leq E_S \\[4ex] \upsilon_{sat} & E \geq E_S \end{cases}
$$

where $\upsilon_{sat} = \mu\, E_S$

* W. Curtice, *IEEE Trans. Electron Devices*, ED-29 (1982) 1942.

The empirical velocity versus electrical field model [*]

$$
v = \begin{cases} \dfrac{\left(\mu + \dfrac{v_{sat}}{E_C} \right) E}{1 + \dfrac{E}{E_C}} & E \leq E_s \\[2em] v_{sat} & E \geq E_s \end{cases}
$$

where $v_{sat} = \mu E_s$

[*] W. Curtice, *IEEE Trans. Electron Devices*, ED-29 (1982) 1942.
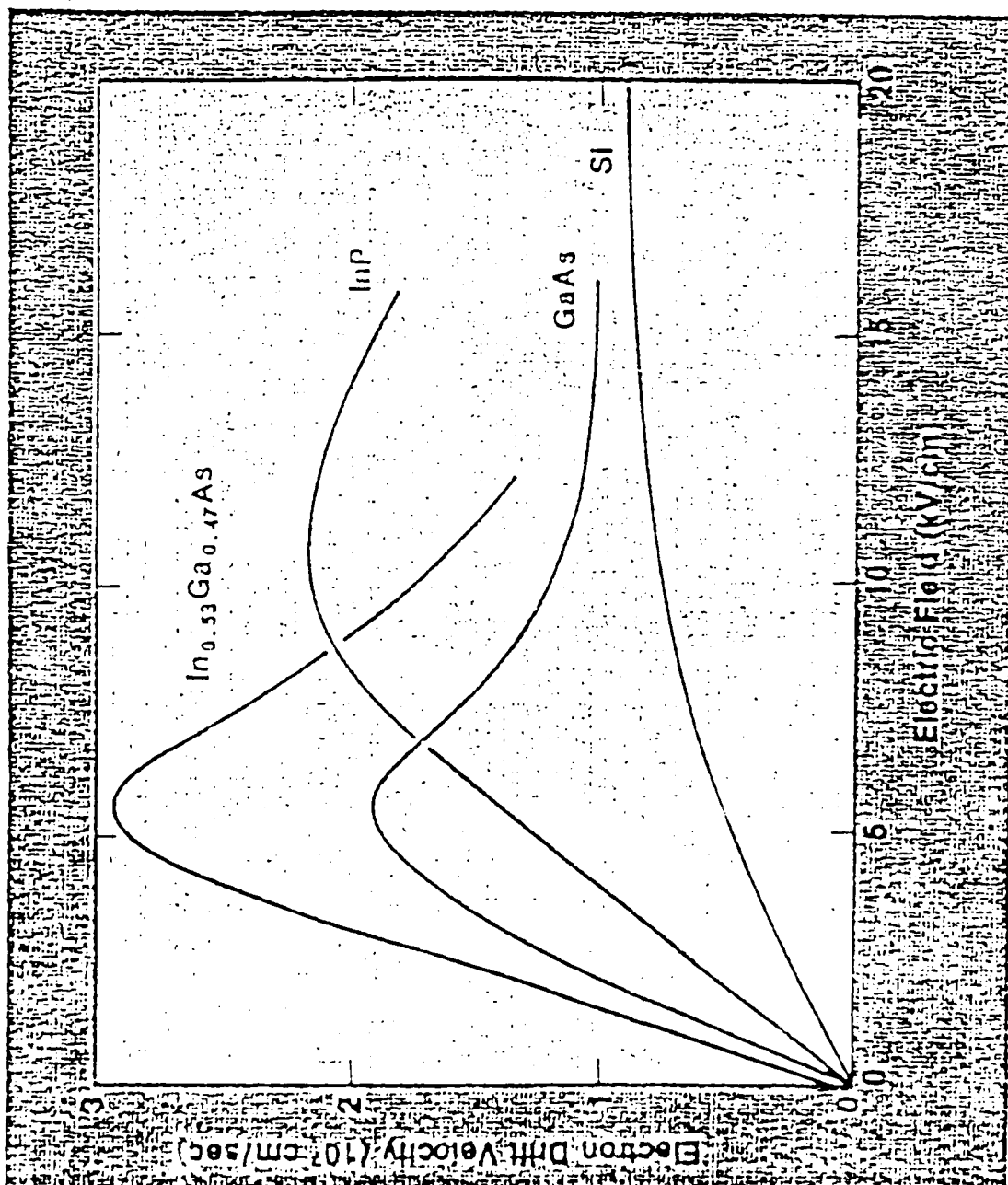
Electric Drift Velocity vs. Electric Field (300 K)

From H. Morkoc et al. Solid State Technology, 31 (1988), 83.

Modeled Drain I – V Characteristics by Variable Interface State Distribution Model
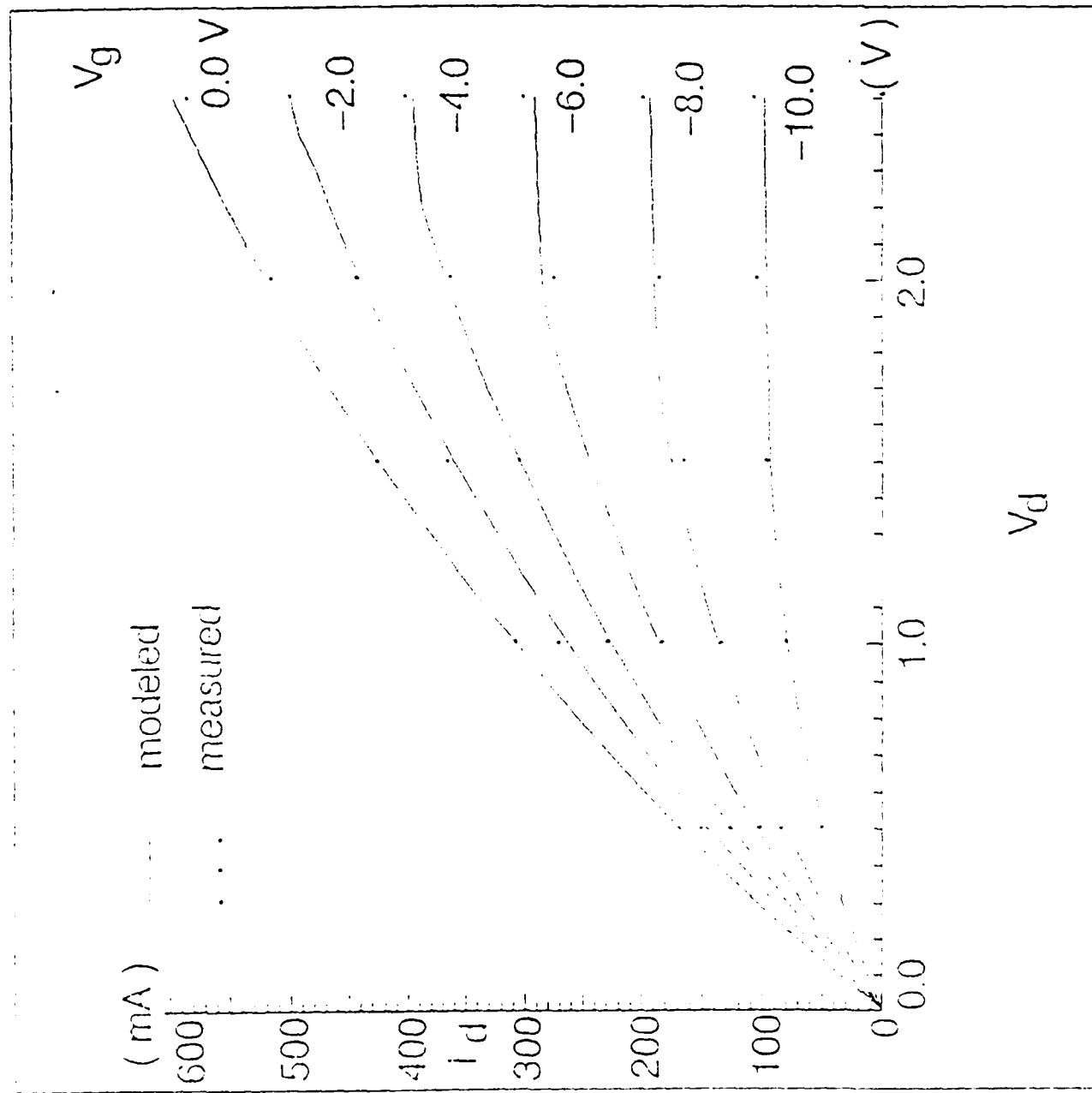
Measured data from L. Messick *et al.*, IEDM (1986) 767.

Modeled Drain I – V Characteristics by Uniform Interface State Distribution Model

Measured data from L. Messick et al., IEDM (1986) 767.
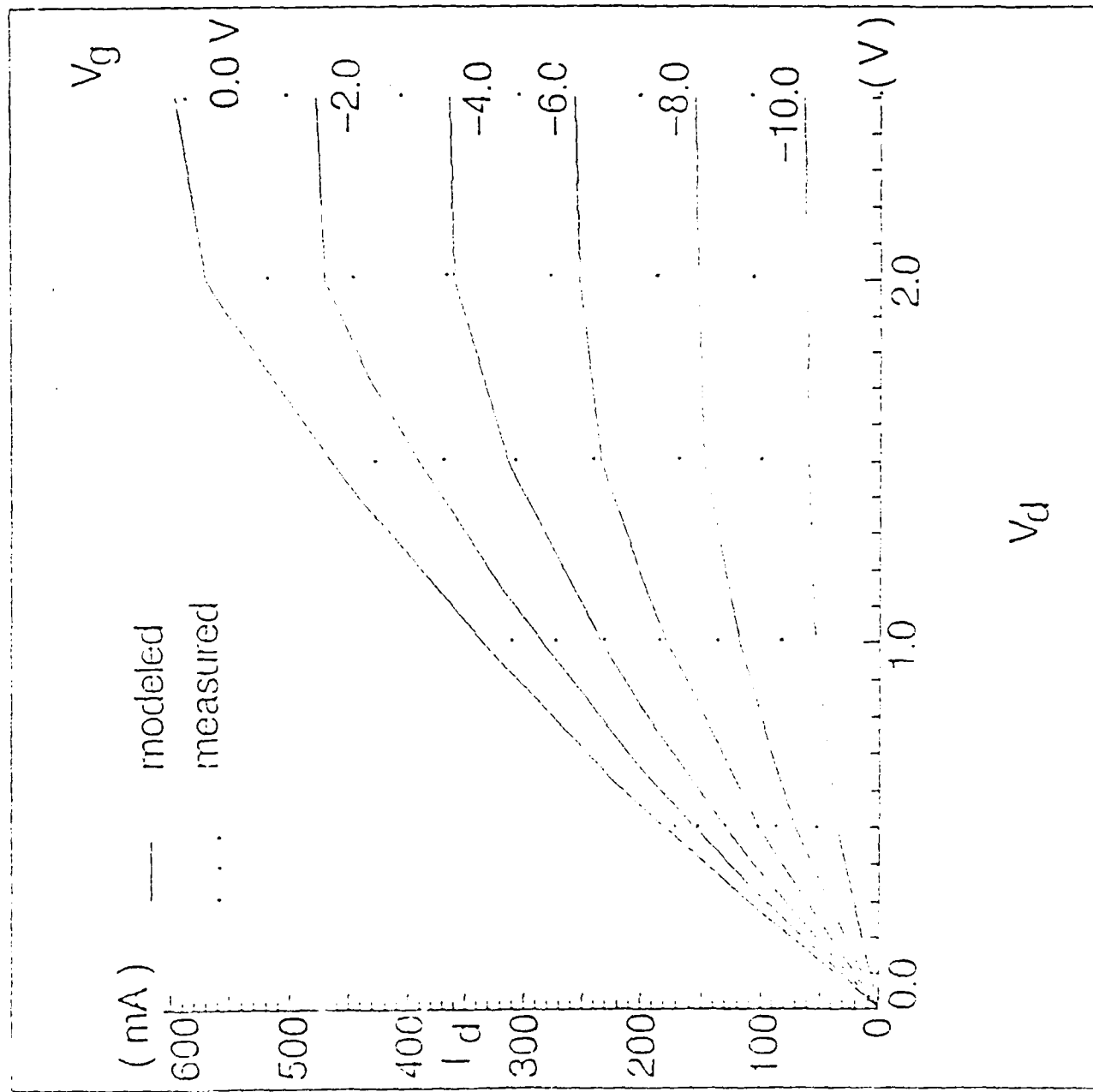
Device parameters used in MISFET models
for the best fit to the measured data

	variable density model	uniform density model	unit
L	1.4	1.4	μm
Z	1000	1000	μm
A	0.2	0.2	μm
t	1000	1000	$\AA$
μ	2000	2000	cm^2 / Vs
E_C	2.0×10^4	2.0×10^4	V / cm
E_S	1.15×10^4	1.15×10^4	V / cm
v_{sat}	2.38×10^7	2.38×10^7	cm / s
ϵ_d	3.9	3.9	ϵ_o
ϵ_s	12.4	12.4	ϵ_o
N_D	1.4×10^{17}	1.4×10^{17}	cm^{-3}
Eg	1.34	1.34	V
ψ_{so}	0.42	0.98	V
N_O	1.2×10^{11}	0	$cm^{-2}eV^{-1}$
E_{oa}	0.11		V
E_O	$Ec - 0.34$		V
Rs	0.6	0.6	Ω
Rd	0.6	0.6	Ω

Two-dimensional Simulation of III–V Compound Semiconductor Devices

Objectives :

- Use two-dimensional simulation to assist in the analysis and modeling of short-channel effects.

- Include momentum balance and energy balance equations to take hot carrier effects into account.

Features :

- New finite-element discretization method [*]

- Fermi-Dirac statistics

- Velocity overshoot effect

[*] W. Ku et al. IEEE Trans. CAD, to appear in May 1989

Simulation Mesh

# of points = 1273

# of elements = 2380

X(μm)
0 3
0 2
0 1
0 0
0

ALGAAS GAAS HEMT SIMULATION

0   1   2   3   Y(μm)
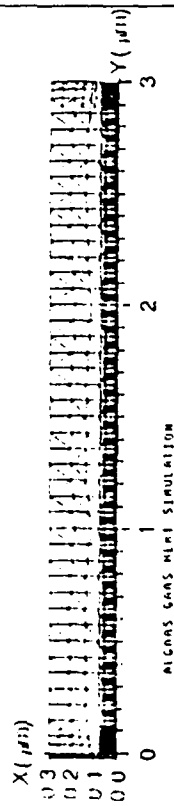
AlGaAs / GaAs HEMT Device Structure Used for Simulation

X(μm)

0.3

0.085

0.055
0.05

0

Source

GaAs   undoped   ← Substrate

GaAs   undoped

$Al_{.3}Ga_{.7}As$ undoped   ← Spacer la

$Al_{.3}Ga_{.7}As$ 5.0×10^{17}

Drain

Gate

0   1   2   3   Y(μm)

Drain I – V Characteristics

I_d (A/cm)

0.2

0.1

0.0

0.1 V

$V_g = 0$ V

−0.1V

0   1   1.7

V_d (V)

ALPHA'S GaAs HEMT SIMULATION

Potential Distribution ($V_g = 0$ V , $V_d = 0.5$ V)

Potential Distribution ($V_g = 0$ V , $V_d = 1.5$ V)
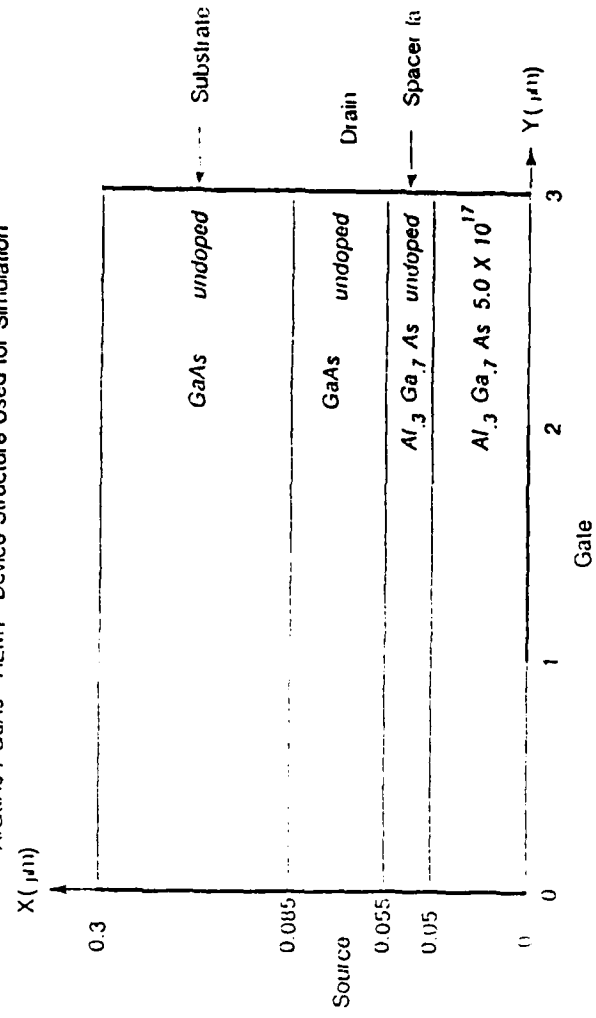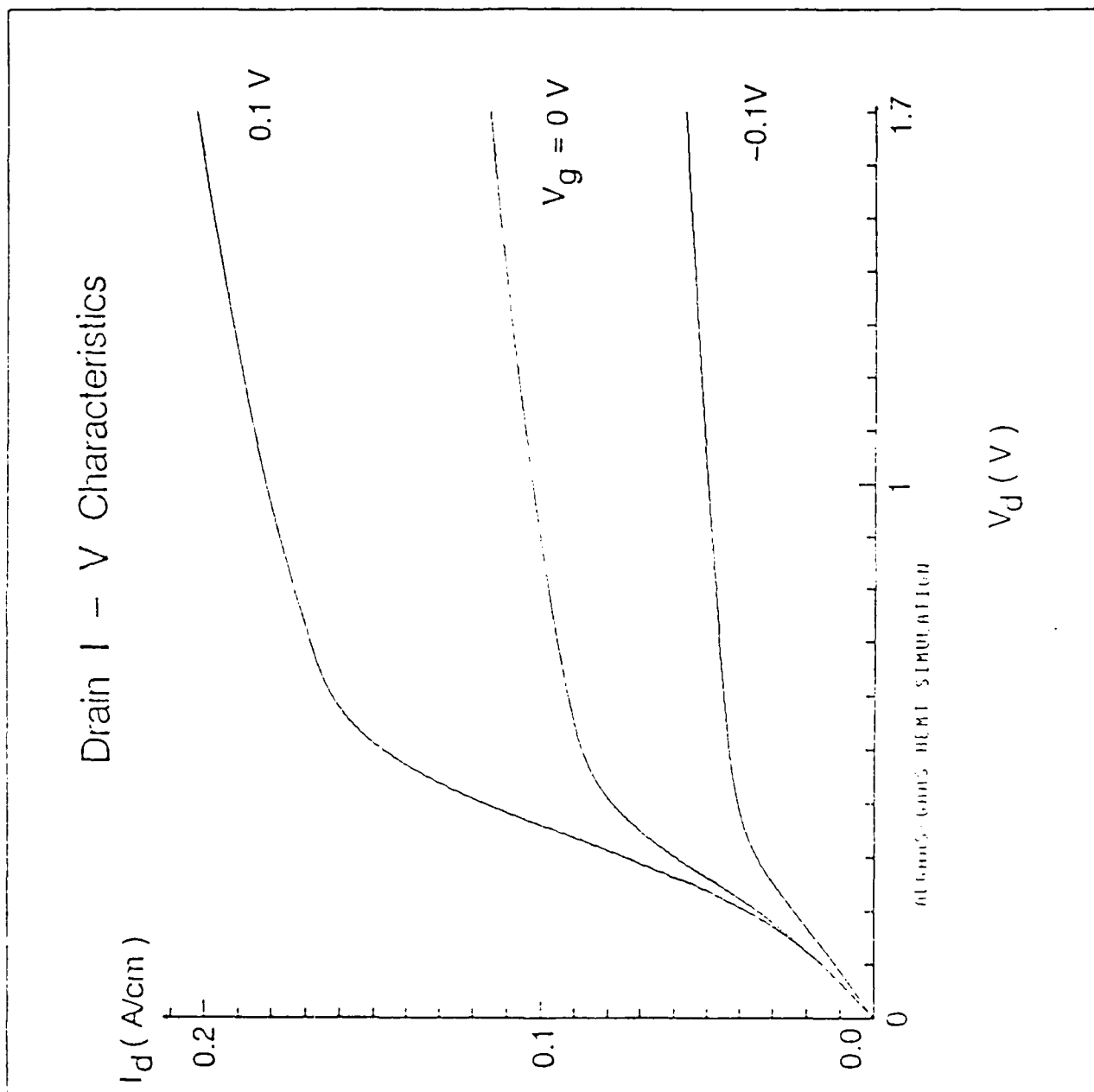
Potential Distribution ($V_g = 0$ V , $V_d = 0$ V)

Potential Distribution ($V_g = 0$ V , $V_d = 10$ V)

Electron Distribution ($V_g = 0$ V, $V_d = 0.5$ V)

Electron Distribution ($V_g = 0$ V, $V_d = 1.5$ V)
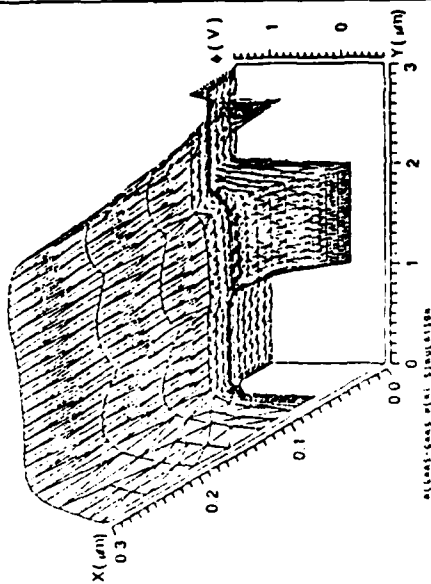
Electron Distribution ($V_g = 0$ V, $V_d = 0$ V)
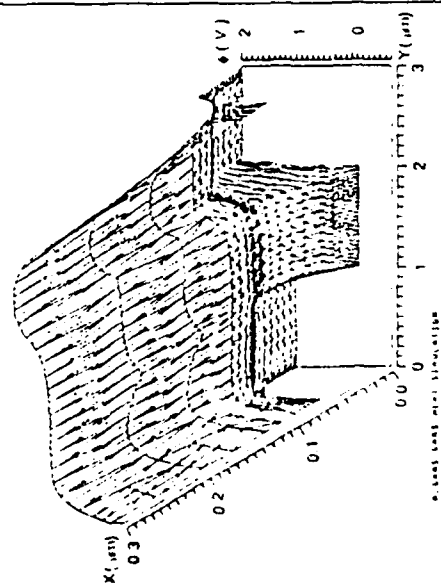
Electron Distribution ($V_g = 0$ V, $V_d = 1.0$ V)
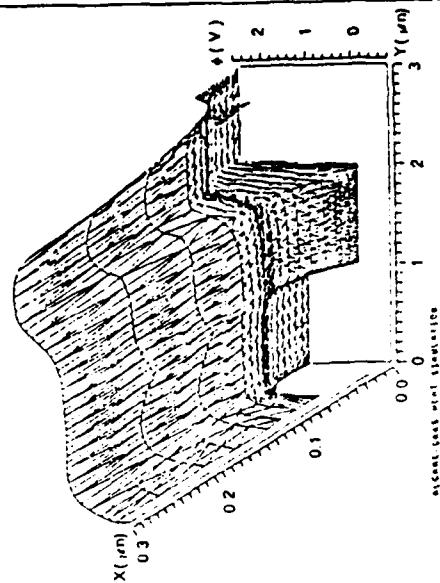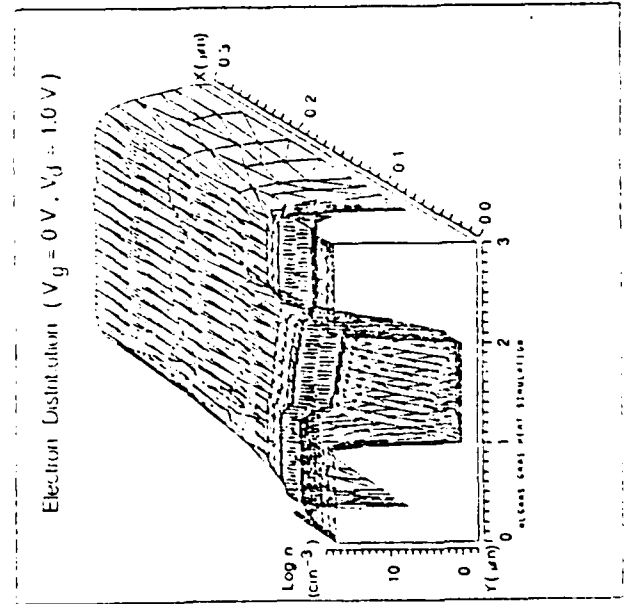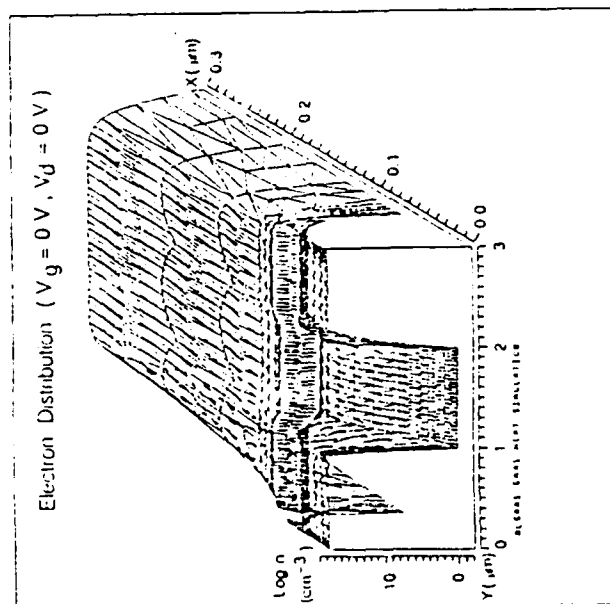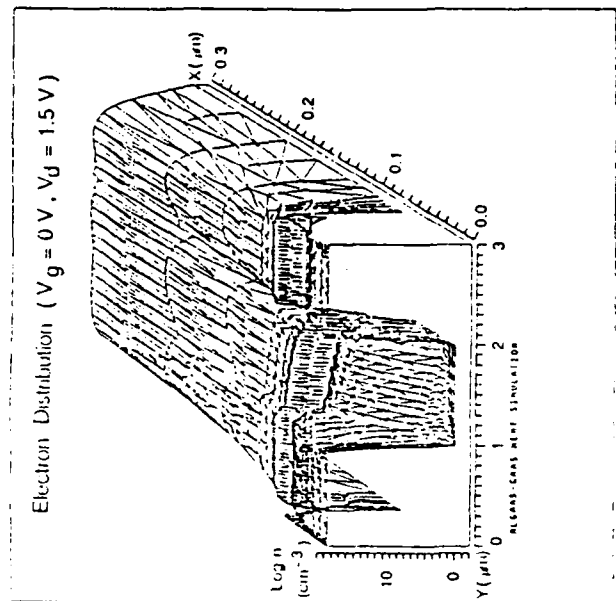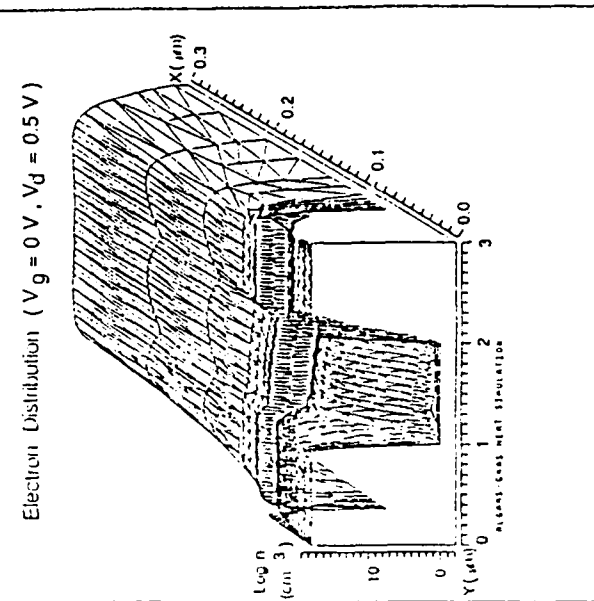
Summary

- The inclusion of interface states distribution profile into drain I – V characteristics model leading to a more accurate description of output performance of MISFETs

- Successful implementation of a two-dimensional model for HEMT devices based on a new finite-element discretization method

- Plan to apply the two-dimensional numerical model to the modeling of submicron gate length MISFETs and HEMTs

A STUDY OF ENHANCED BARRIER SCHOTTKY GATES FOR N-InP MESFETS

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Columbia, MD

241
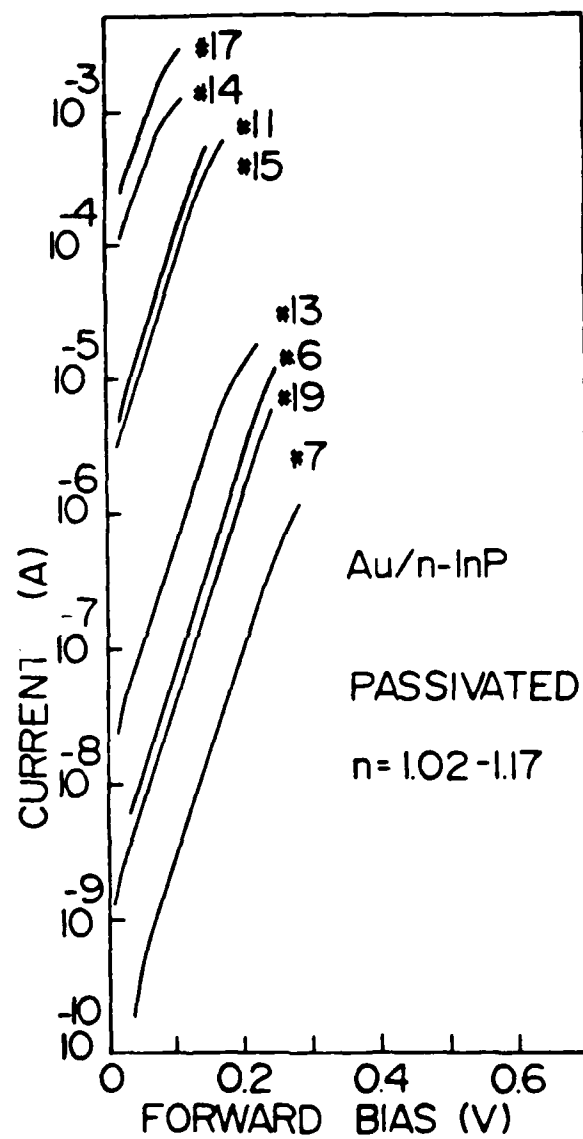
Fig. 1
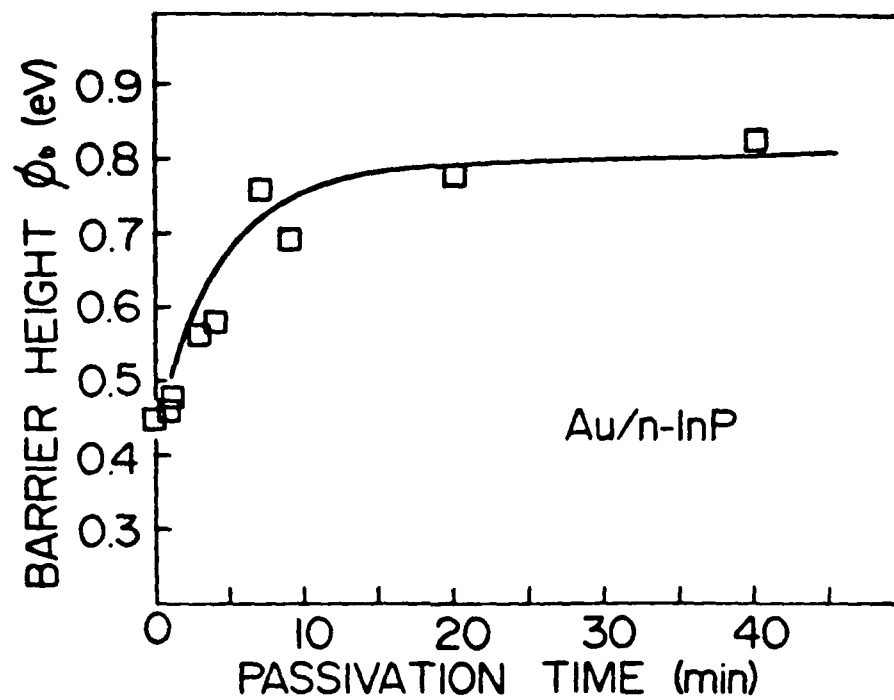
Fig. 2
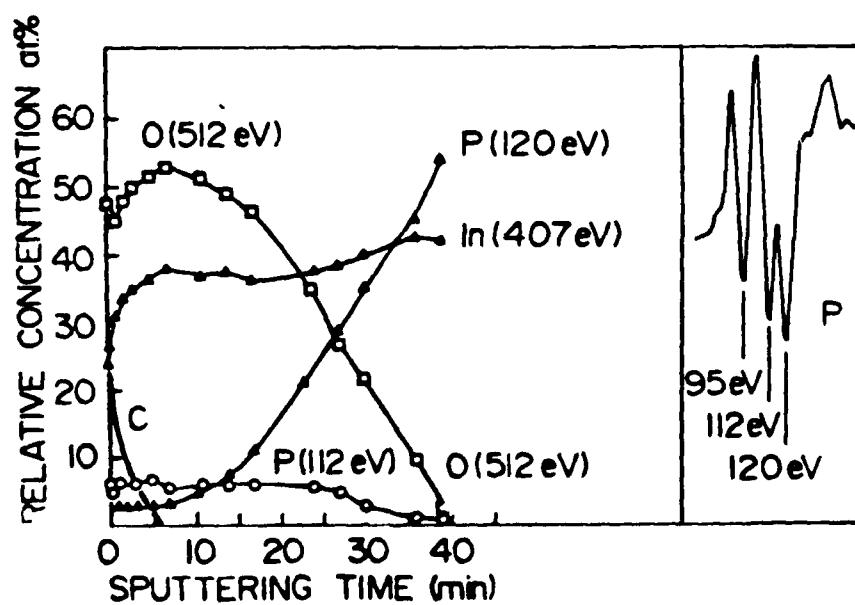
Fig. 3
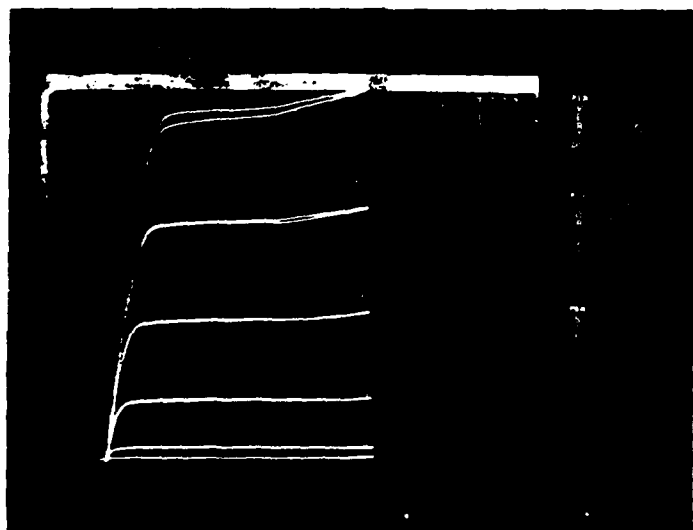
Fig. 4.

FIGURE CAPTIONS

Figure 1. Family of forward I-V characteristics of diodes passivated for various times.

Figure 2. Barrier height Φ_b versus the passivation time. A gradual increase of Φ_b with passivation time is evident in this figure.

Figure 3. Auger depth profile of the InP surface after paassivation. The inset of the figure shows the Auger peaks of oxidized phosphorus at 95 eV and 112 eV and elemental phosphorus at 120 eV. A phosphorus oxide is dominant in this profile.

Figure 4. Drain current-voltage ($I_{ds} - V_{ds}$) characteristics of a transistor with a peak transconductance of 60 mS/mm.

RESEARCH ON InP DEVICES AT LINCOLN LABORATORY

A. R. Calawa, C. L. Chen, J. D. Woodhouse, S. C. Palmateer, S. H. Groves,
G. W. Iseler, W. E. Courtney, and J. P. Donnelly

Lincoln Laboratory
Massachusetts Institure of Technology
Lexington, MA 02173-0073

RESEARCH ON InP DEVICES AT LINCOLN LABORATORY*

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Introduction

For over two decades GaAs was considered the electronic material of the future. Even today some researchers feel it will always be the material of the future, although significant commercial markets have been found for LED's and to a lesser extent for diode lasers and integrated circuits. The use of InP as an electronic material has faced even more severe rejection in spite of the clear advantages offered by its electronic properties. Recently, however, interest in InP has been increased by the demonstration of high-performance InP MISFETs and InGaAs HEMTs and HBTs fabricated on InP substrates.

Lincoln Laboratory has been working on InP and InP-based devices for over 20 years, nearly as long as on GaAs-based devices. For example, Lincoln played a pioneering role in the development of GaInAs/InP diode lasers used in optical fiber communications. The Laboratory has equipment for vertical-gradient-freeze and liquid-encapsulated-Czochralski crystal growth capable of producing semi-insulating Fe-doped InP crystals with a resistivity greater than $10^7 \Omega$cm. Organometallic vapor phase epitaxy (OMVPE) has been used to grow InP epilayers, on InP substrates, with a carrier concentration of 9×10^{13} cm^{-3} and mobility of 68,000 cm^{2}V^{-1}s^{-1} at 77K. Recently, InP with a carrier concentration of 1×10^{15} cm^{-3} and mobility of 25,000 cm^{2}V^{-1}s^{-1} at 77K has been grown by OMVPE on GaAs substrates. We believe that the interim acceptance of InP devices may depend on the ability to integrate InP and GaAs.

Our interest in InP transistors has been spurred by the great success achieved by Thompson-CSF and NOSC in using the InP MISFET as a microwave power amplifier. We believe that this device is a significant competitor to the GaAs permeable base power transistor being developed at Lincoln Laboratory. As a result, over the past two years a small effort has been devoted to the development of InP FET's. The high-frequency performance of fully implanted p-column FET's and of p^+-AlInAs/InP junction FET's made by

selective molecular beam epitaxy has been reported previously. Recently we have begun to investigate SiO_2-insulator MISFETs. Devices with gate length and gate width of 1.5 µm and 500 µm, respectively, have delivered 860 mW of output power at 5 GHz with a power-added efficiency of 32.5%. Their f_{max} is typically 18 GHz. We find these results particularly encouraging because these devices do not incorporate a number of features that can be expected to improve their stability and performance. We will discuss some of these features, including improvements in device geometry and SiO_2/InP interface quality, from a different perspective than previously employed. The outline of this talk is given on Slide 1. Although I have divided the talk into three parts, I intend to spend only two to three minutes on the first two parts and the remainder of the time on very recent work on the development of the InP MISFET.

History

InP research at Lincoln Laboratory, actually started in the late 1950's, the time when it was fashionable to work on determining the band structures of various semiconductor materials. It wasn't until the early to mid 1960's that the first InP device, the homojunction laser, was developed. Interest in InP was spurred with the development of the Gunn diode which was more efficient than that in GaAs and with the development of the InGaAsP quaternary heterojunction laser.

Slide 2 outlines the Laboratory's areas of interest and the participant researchers throughout the 1970's and 80's. The interesting fact to be observed here is that, of all the devices developed, only the quaternary laser has attracted commercial interest which resulted in the start-up of Lasertron, a company which manufactures these lasers.

All of the InP microwave transistor research at Lincoln Laboratory was performed within the past two years and is outlined on Slide 3. J. D. Woodhouse and J. P. Donnelly devoted only a small fraction of their time on this work and published the two JFET papers listed here. Although these devices are state-of-the-art, they offer no competition to GaAs devices. The InP MISFET is, however, quite a different matter. With three times the power handling capability of GaAs microwave devices operating at the same frequency and nearly twice the efficiency, the InP MISFET cannot be ignored. The remainder of this talk will be devoted to our efforts to fabricate this device in the past few months.

Current Research

Slide 4 is a photograph of one of the first InP power MISFETs that we have constructed. The photolithography mask set used to fabricated this device was designed for the fabrication of a 2 GHz GaAs power MESFET, and is not considered an optimum structure for the InP MISFET. The objective in building this device was to determine how difficult it would be to achieve near state-of-the-art power performance, and to investigate the reported problem areas of the device by analyzing its DC and RF output characteristics. The active channel of the device consists of an OMVPE grown n-type InP epilayer with a carrier concentration of 2×10^{17} cm^{-3}. An n$^+$ cap was also grown to improve the source and drain contact resistances. After applying the source and drain contacts, the gate region was chemically recessed to obtain the desired drain current. A 20Å Si layer was deposited over the gate region followed by a standard pyrolytic oxide grown at about 400°C. The reason for the Si layer will be made clear in my discussion on insulators. The gate length and width of the device are 1.1 μm and 500 μm respectively. This device had an output power of 850 mW at 5 GHz with an associated gain of 4 dB. The output power of nearly 2 W/mm of gate width was obtained with a power added efficiency of 32%. These characteristics are plotted as a function of drain voltage on Slide 5. While this output is about a factor of two less than the best reported value for InP MISFETs, it is considerably better than that achieved with any GaAs devices. Both of the InP MISFET problems of drain current drift and catastrophic burnout were observed in this device. These are outlined in Slide 6. The drift in drain current over time when the drain bias is constant has been attributed to traps in the gate insulator. By properly depositing the insulator at low temperature, the drain current drift can be reduced to a few percent over many hours of operation.

The catastrophic burnout occurs when the RF power input to the transistor is turned off before the drain voltage is turned off. If the drain voltage is turned off prior to turning off the the RF input, the device is not harmed. We believe some information may be gained regarding burnout by observing the frequency dependence of three-terminal transistor characteristics. These are shown on the Slide 7

The current-voltage characteristics were taken point by point at 400 Hz and 20 kHz. A 12.5 Ω drain-load resistor was used. Two factors are immediately

obvious. The transconductance is higher and the device is capable of withstanding a considerably higher drain-source voltage (V_{ds}) at the higher frequency. Note that the drain-source breakdown occurs at a much lower voltage for the low frequency drive, particularly near pinch-off. Clearly, the frequency dependence indicates that slow traps are responsible for the observed effect. The data also suggest that the traps may be in the buffer layer and not in the oxide as one would suspect. This is consistent with previous observations that decreasing drain current drift which is known to be related to states at the gate insulator-semiconductor interface, does not cure or even lessen the burnout problem.

Our approach to minimizing surface states or traps at the gate insulator-InP interface is illustrated in the next few slides. We believe that during the deposition of any insulator on InP several distinct layers are likely to form in the InP. Schematic representations of these interface layers are shown in Slide 8. Evidence for the existence of these layers has been provided by high resolution transmission electron microscopy. The reason multilayers form is well known. Virtually any heating of the InP will cause the loss of P and any exposure to air (even at room temperature) will cause the surface material to oxidize. The figure on the left illustrates what will likely happen if SiO_2 is deposited onto InP. The degree to which this will happen depends on the deposition temperature. The energy band diagram below the figure illustrates the trapping states which could occur in such a layered configuration. Obviously this diagram is idealized in that there will surely be an intermixing of the layers. Also, the conduction band discontinuities between these layers are not known. Still the model bears some merit. In losing phosphorus the surface of the InP will be In rich and oxides of In will form. The InP below that layer should be stoichiometric and the oxide is likely to become $InPO_4$. The most common In oxide, In_2O_3, is known to be conducting and $InPO_4$ is insulating which is consistent with diagram shown. In the middle figure, SiO_2 has been deposited on sulfurized InP. The In_2S_3 and $InPS_4$ which are believed to be formed, are semiconductors with band gaps of 2 eV and 3.4 eV respectively. The resulting conceptual band diagram is shown below the figure. Again the possibility of trapping at this interface is evident. The figure on the right assumes that the InP is sulfurized in the presence of a high phosphorus overpressure. This would be analagous to the oxidation of Si where a clean interface could be maintained. That, however, is as far as the analogy would go. The dielectric breakdown strength of $InPS_4$ is considerably

less than that of SiO_2, therefore the layer thickness required is much greater. This would lower the gain of the MISFET. The higher dielectric constant of $InPS_4$ (e_r = 9.4) would result in a higher gate capacitance and lower operating frequency.

Slide 9 represents an alternative approach for depositing a stable SiO_2 layer while reducing the semiconductor oxides. The depletion-mode GaAs MISFET was recently revived when a thin Si layer was placed between the GaAs and SiO_2 insulator. Apparently this layer decreased the GaAs surface state density to the point where the Fermi level at the GaAs-SiO_2 interface became unpinned. The role of the Si remains unexplained. We suggest that the Si may act as a getter for oxygen and that some of the surface states may be due to oxides of Ga or As. We also suggest that the same process may work for InP if proper procedures are employed. In the proceedure we have employed, Si is deposited by molecular beam epitaxy (MBE) onto an InP surface which has been exposed to air. The wafer is then annealed at sufficiently high temperature to reduce the InP oxides. From our experience with MBE growth on InP surfaces this temperature is known to be in the range of 500-550°C. Free In should either react with the phosphorus (if a phosphorus overpressure is used in the annealing) or vaporize from the SiO_2 surface. The annealed layer is depicted in the diagram on the right. In this case a very small amount of $InPO_4$ remains. Whether this would be more desirable than having an excess of Si at the interface is not clear, but either structure could be achieved by adjusting the amount of Si deposited. We believe the resulting structure would be stable at all subsequent processing temperatures. Auger profiles of our first attempt at producing such a structure are shown on Slide 10.

About 40Å of Si was evaporated in an MBE system with a base pressure of 5×10^{-10} Torr onto an OMVPE grown InP epilayer which had been exposed to air at room temperature for about two hours after removal from the OMVPE reactor. The wafer was removed from the MBE system after the Si deposition and exposed to air for about one hour before loading into an OMVPE system for annealing. The wafer was then annealed at 600°C for 30 minutes with the same phosphine flow used in that reactor to grow high quality InP. H_2 was the carrier gas used in the OMVPE reactor which may be undesireable because of its tendency to reduce SiO_2. The wafers were exposed to air at room temperature for three days prior to taking the Auger profiles. These data were obtained from the constituent element profiles by assuming that the only material remaining at the end of the sputtering was stoichiometric InP, and by

normalizing the Auger traces to these values. Since these are the first profiles obtained, we hesitate to draw too many conclusions. Still, the profiles are in agreement with our expectations. In the upper traces it appears that the excess In magnitude and the depth of the region of excess In are reduced after annealing. In the lower traces it appears that the oxygen is accumulating at the surface. This is also predicted by the model assuming the oxygen is gettered by the Si. Ti-Au dots were evaporated onto the annealed and unannealed layers in an attempt to obtain C-V profiles. In each case the surface layers were too thin to sustain the required voltages. However, the resistance of the annealed layer was about 5 times greater than that of the unannealed layer.

In conclusion, we feel that the success of the InP MISFET will play a very significant role in the acceptance of InP IC's. Devices like the InP MISFET which are not merely marginally better than GaAs devices intended for the same use, but 2-3 times better, will accelerate the acceptance of the material. We have shown that a thin layer of Si between the InP channel layer and an SiO_2 gate oxide is beneficial in reducing drain current drift and have presented a model for the interface reaction. We believe that the optimization of this structure will significantly reduce the InP MISFET problems.

OUTLINE

InP DEVICE RESEARCH AT LINCOLN LABORATORY

- PAST AND PRESENT OPTOELECTRONIC DEVICE INTEREST

- InP MICROWAVE TRANSISTOR TECHNOLOGY

- CURRENT InP MISFET RESEARCH

(WILL InP IC's EVER MAKE IT?)

InP OPTOELECTRONIC DEVICE INTEREST

1970 - 1989

CRYSTAL GROWTH

G.W. ISELER	LEC substrates
S.H. GROVES	LPE, MOCVD
J.J. HSIEH*	LPE
Z.L. LIAU	LPE
S.C. PALMATEER	MOCVD
A.R. CALAWA	MBE

DIODE LASERS AND ARRAYS

J. ROSSI*	Z.L. LIAU
J.J. HSIEH* (Lasertron)	D.Z. TSANG
J.N. WALPOLE	V. DIADIUK

OPTOELECTRONIC SWITCHES

A.G. FOYT*	C.H. COX
F.J. LEONBURGER*	R.C. WILLIAMSON
V. DIADIUK	

DETECTORS

C.E. HURWITZ*	V. DIADIUK
R.H. KINGSTON*	J.P. DONNELLY

SOLAR CELLS

G.W. TURNER

* No longer at Lincoln Laboratory

Slide 2

InP MICROWAVE TRANSISTOR TECHNOLOGY

1986 -1988

MICROWAVE TRANSISTORS

J.D. WOODHOUSE
J.P. DONNELLY

"Fully Implanted p-column InP Field-Effect Transistor",
J.D. Woodhouse and J.P. Donnelly, IEEE Electron Device Letters EDL-7,
387 (1986)

"p+ -AlInAs/InP Junction FET's by Selective Molecular Beam Epitaxy"
J.D. Woodhouse, J.P. Donnelly, M.J. Manfra, and R.J. Bailey, IEEE
Electron Device Letters 9, 601 (1988)

RESONANT TUNNELLING OSCILLATORS

E.R. BROWN
T.L.C.G. SOLLNER
A.R. CALAWA
C.L. CHEN

InP MICROWAVE TRANSISTOR TECHNOLOGY

1986 -1988

MICROWAVE TRANSISTORS

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A.R. CALAWA
C.L. CHEN

InP MISFET POWER VS DRAIN VOLTAGE

Slide 5
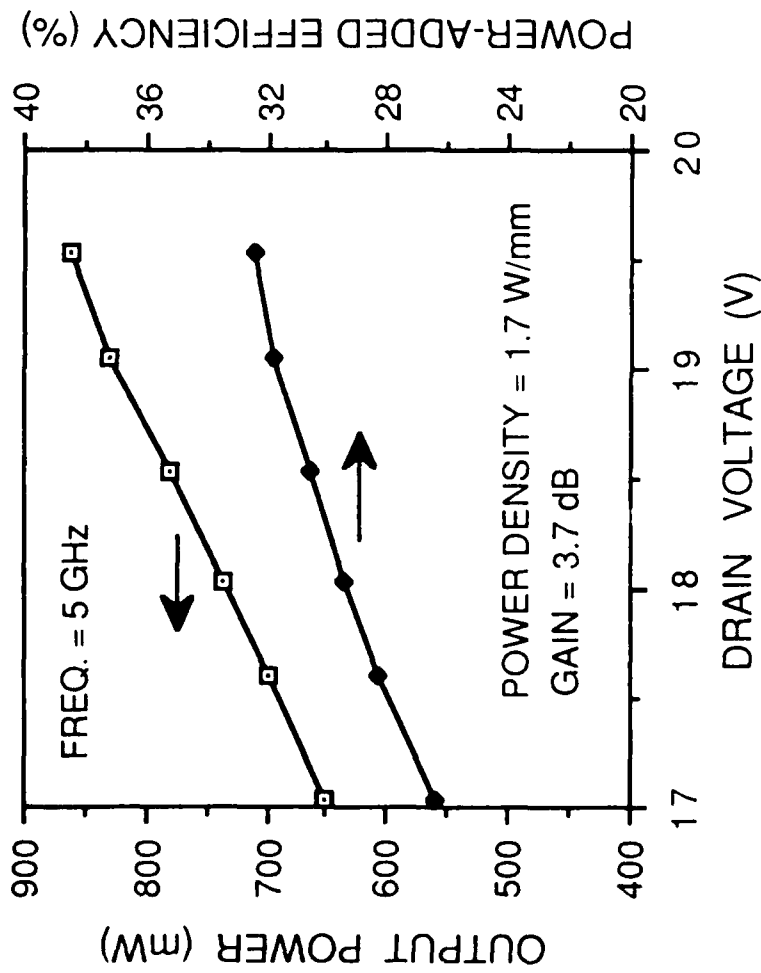
TWO MAJOR PROBLEMS WITH InP MISFETS

- ## DRAIN CURRENT DRIFT

  1) DEFINITELY INSULATOR RELATED

  2) LESS THAN 4% IN 2 HRS FOR OUR DEVICE
     (20 KHz, 4 V PEAK-TO PEAK GATE DRIVE)

- ## CATASTROPHIC BURNOUT

  1) OCCURs IF V_g (RF) IS TURNED OFF BEFORE V_{ds}
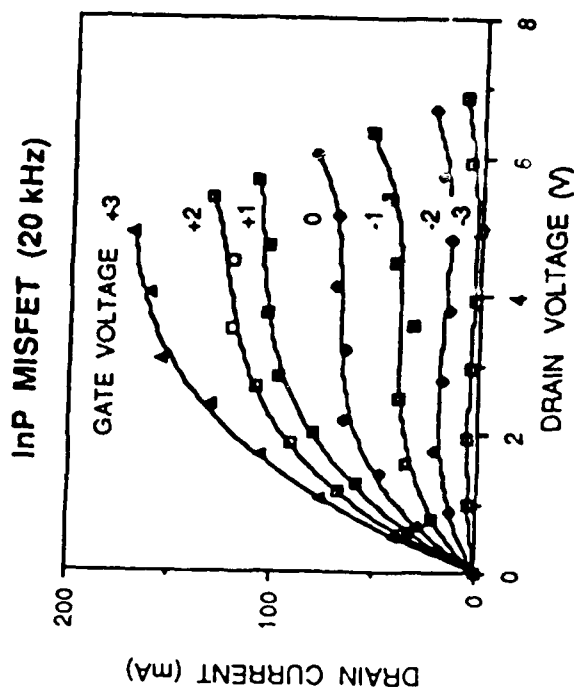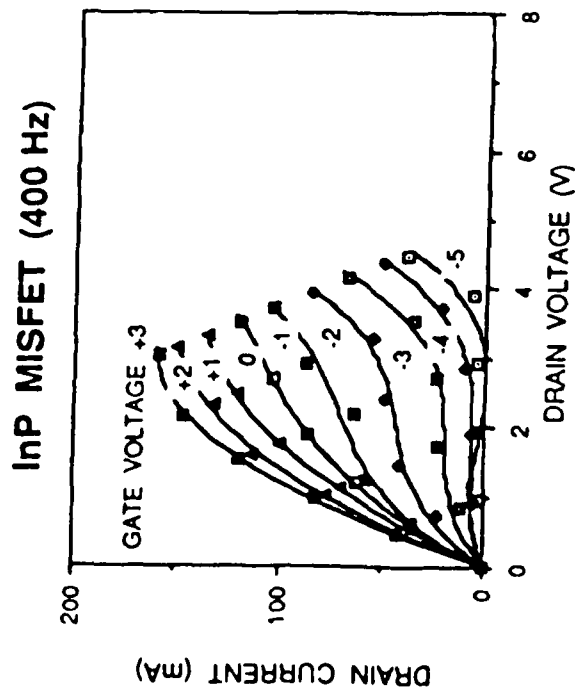
  2) MAY NOT BE RELATED TO DRAIN CURRENT DRIFT

  3) POSSIBLE CAUSES:
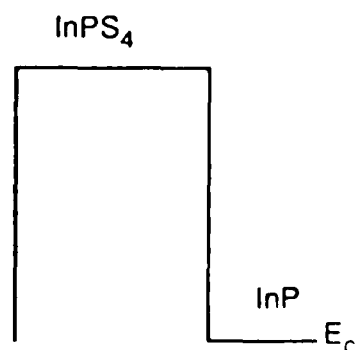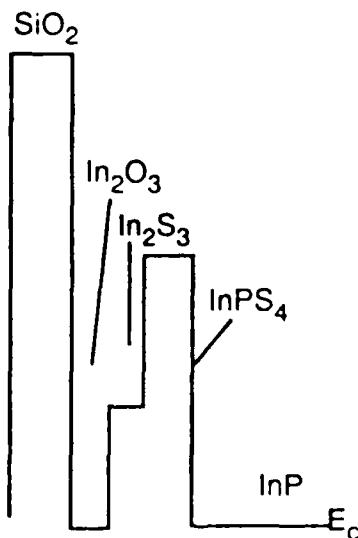
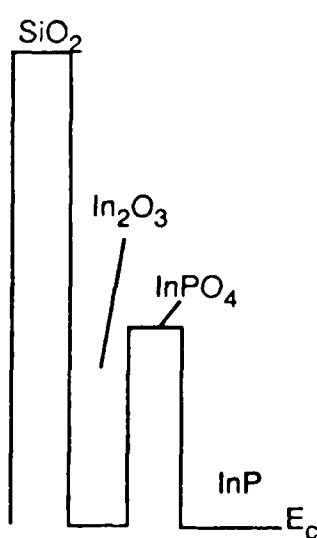   a) Slow moving positive charge at oxide-InP interface

     b) Slow responding traps in Fe-InP buffer

Slide 6

FREQUENCY DEPENDENCE OF CURRENT-VOLTAGE CHARACTERISTICS

Slide 7

PUTTING INSULATORS ON InP
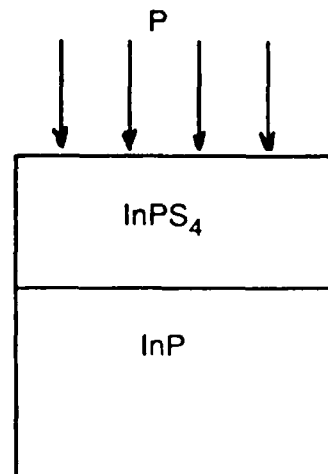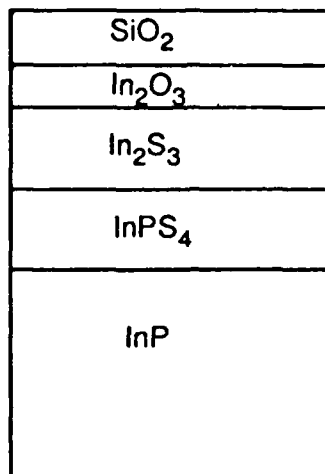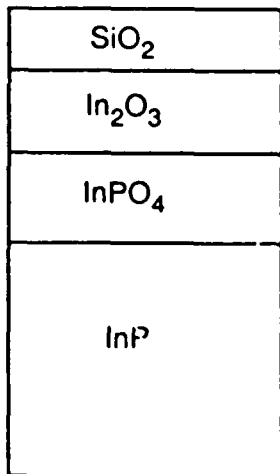
For evidence of multilayer structures formed at SiO2 / InP interfaces see:
"High-Resolution Microanalysis of Semiconductor Interfaces", O.L. Krivanek and
Z. Liliental, Ultramicroscopy 18, 355 (1985)

"Native oxide formation and electrical instabilities at the InP interface"
J.F. Wager, K.M. Geib, C.W. Wilsem and L.L. Kazmerski, J. Vac. Sci. Technol. B1
778 (1983)

Slide 8

262

OXYGEN GETTERING AT InP - SiO$_2$ INTERFACES

$$2 \, In_2O_3 + 3 \, Si + 4 \, P \quad \text{-----------} \rightarrow \quad 3 \, SiO_2 + 4 \, InP$$
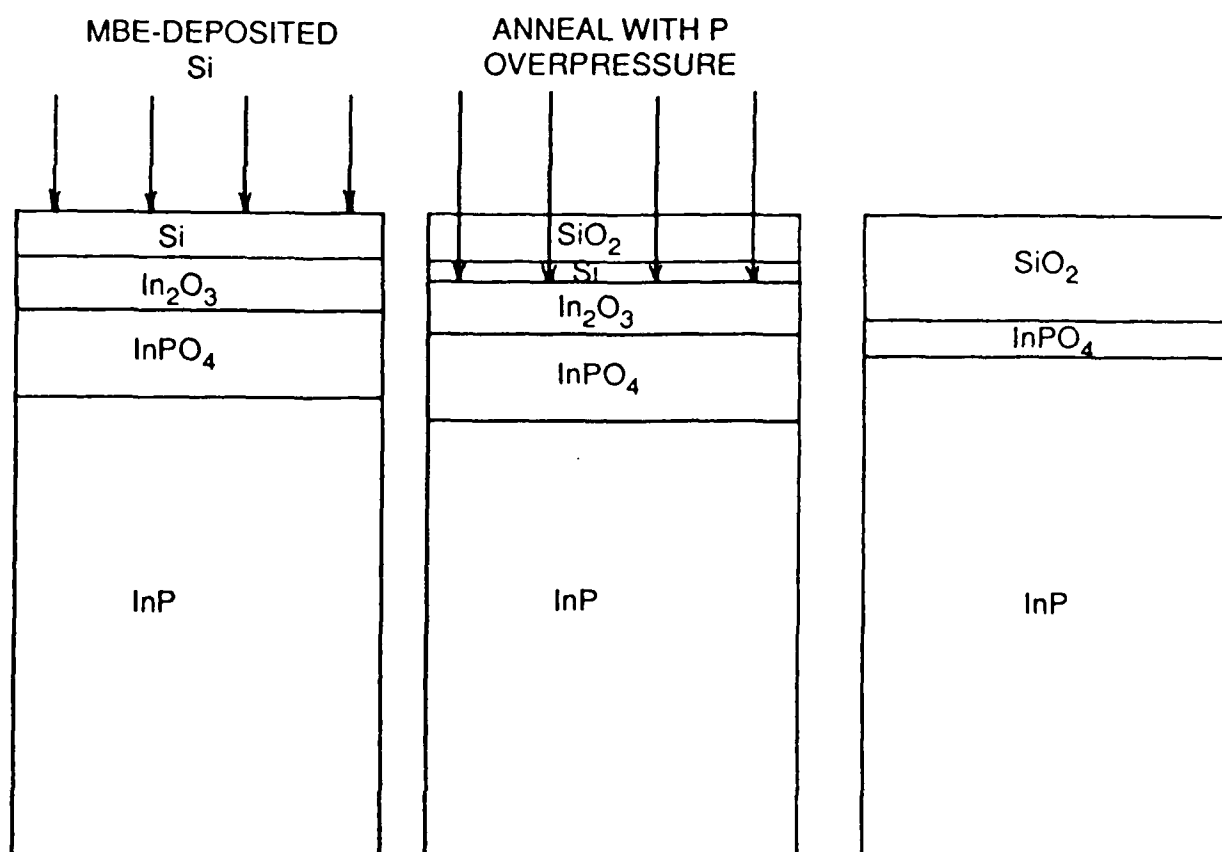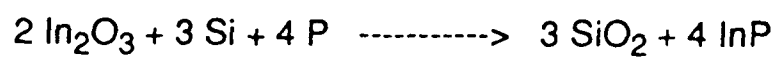
AUGER PROFILES OF Si COATED InP
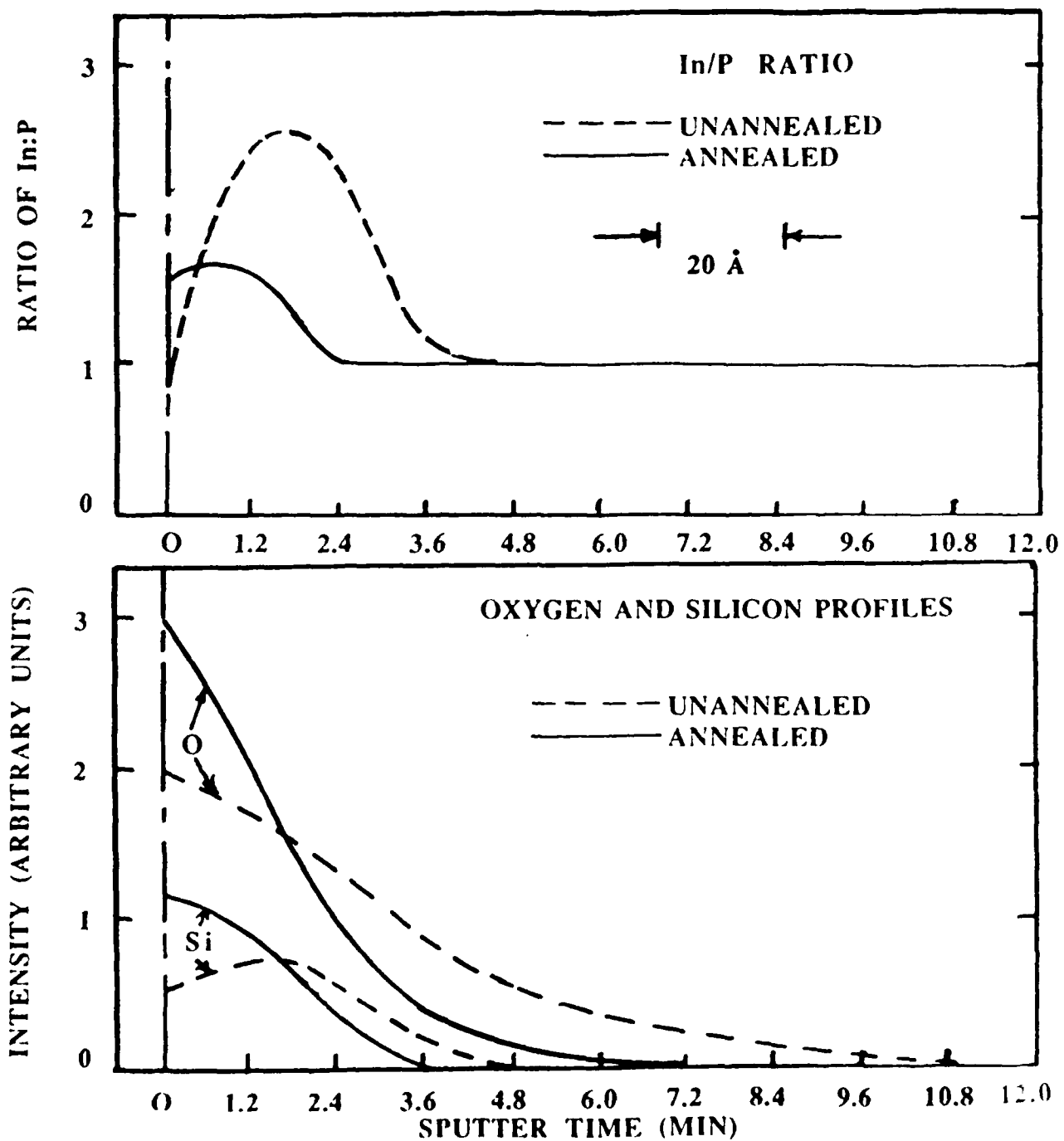
Slide 10

HIGHLY STABLE InP/InGaAs HETEROSTRUCTURE INSULATED-GATE FETS

Eric A. Martin*, Leye A. Aina, Agis A. Iliadis♦,
Mike R. Mattingly, and Erica Hempfling

Allied Signal Aerospace Company
Aerospace Technology Center
9140 Old Annapolis Road
Columbia, MD 21045

♦University of Maryland
Electrical Engineering Department
College Park, MD 20742

*also with the University of Maryland, Electrical Engineering Department
College Park, MD 20742

Highly Stable InP/InGaAs Heterostructure Insulated-Gate FETs

Eric A. Martin,[*] Leye A. Aina, Agis A. Iliadis,[†]
Mike R. Mattingly, Erica Hempfling

Allied-Signal Aerospace Company, Aerospace
Technology Center,
9140 Old Annapolis Road, Columbia, MD 21045

[*]also with the University of Maryland, Electrical
Engineering Department, College Park, MD 20742

[†]University of Maryland, Electrical Engineering
Department, College Park, MD 20742

Outline

- Motivation/Justification for InP/InGaAs HIGFETs

- Gate Insulator Technologies: SiO_2 and InAlAs

- DC Characterization - high transconductance

- Reduced Drain-Current Drift

- Microwave Characterization

- Summary and Future Work

MOTIVATIONS FOR HIGFET RESEARCH

- **Favorable Electrical Properties of InP/InGaAs: high μ, v_{sat}, large Γ-L separation**

- **Resulting Expectations of High Performance FETs: high g_m and f_{max}, large BV_{GD}, low access resistance** ·

- **Opto-electronic compatiblity with InP/InGaAs-based photodetectors and sources**
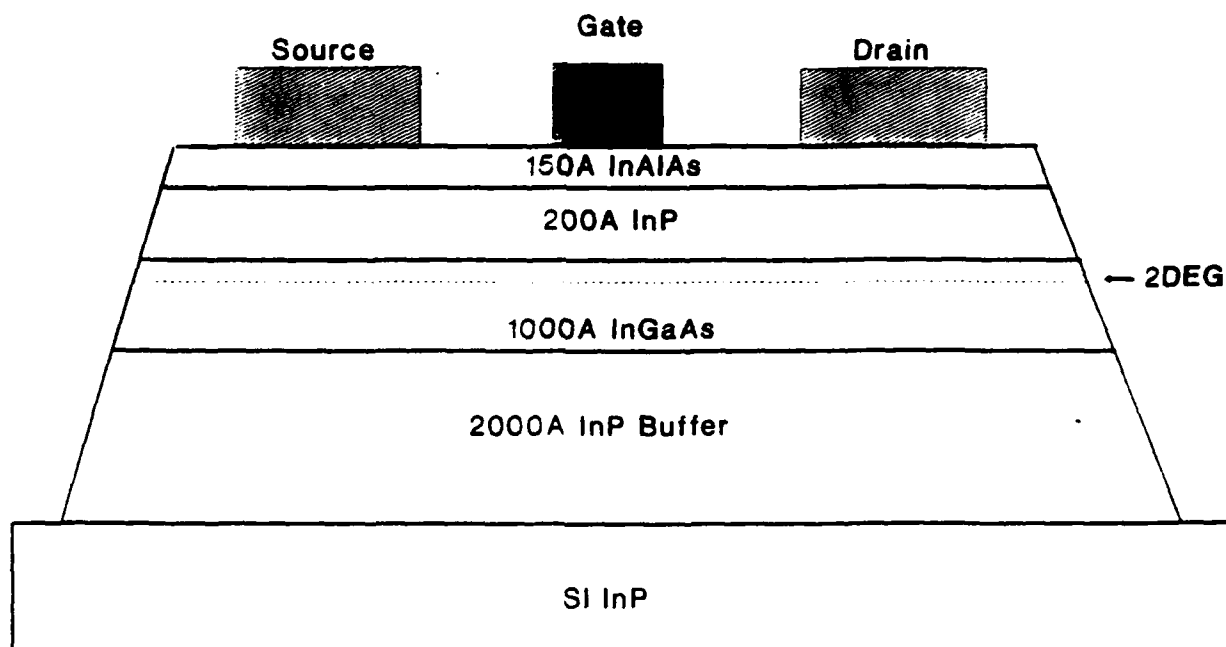
InAlAs-Based HIGFET Cross-Section

- All layers **undoped**, lattice-matched; InP/InGaAs heterojunction channel

- In-situ-grown $In_{0.52}Al_{0.48}As$ gate insulator (15 nm)

- $3\mu m$ source-drain spacing, $1\mu m$ gate length

InAlAs-Based HIGFETs: Progress

- **High Transconductance**: 566 mS/mm (300K; unstable at 77K)

- **No Drain-Current Drift**

- **High Output Condutance** $g_o = 50$ mS/mm

- **Voltage Gain** $g_m/g_o = 10$

- **Threshold Voltage** ($V_t = -2.5$V [300K])

- **Breakdown Voltage** as large as 8-10V. 1-2V for high gain devices

#263: InAlAs-based HIGFET
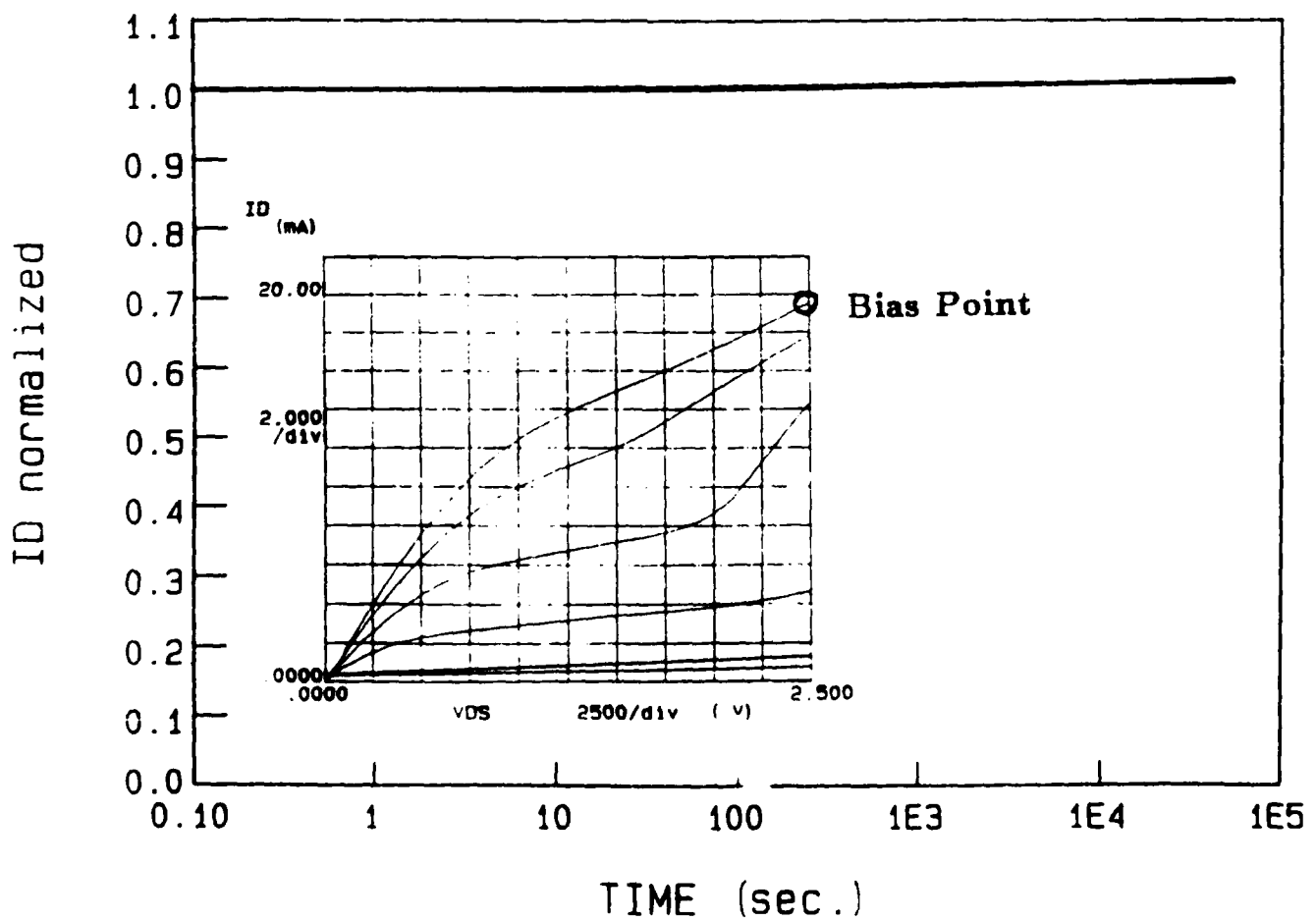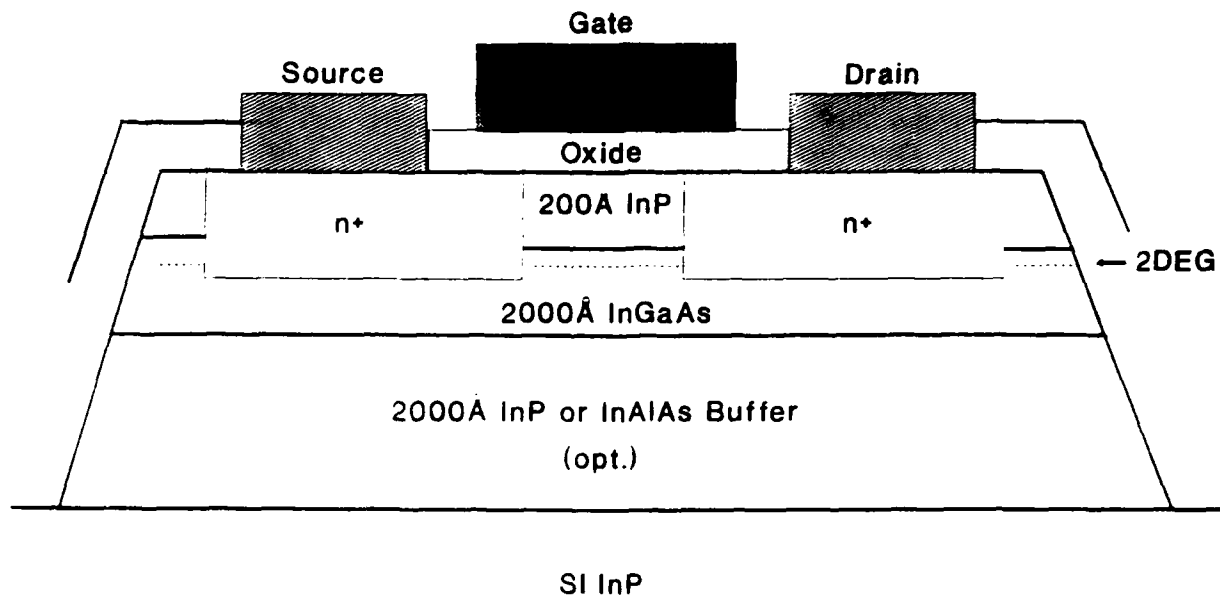
SiO$_2$-Based HIGFET Cross-Section

- <u>Undoped</u>, lattice-matched InP/InGaAs heterojunction channel

- PECVD-deposited SiO$_2$ gate insulator (30-60 nm)

- Implanted Si^{29} source/drain

SiO$_2$-Based HIGFET Summary

- Good DC Gain $g_m/g_o = 260/18 = 14$

- Very Large $BV_{GD} > 20V$

- I_{DS} at peak transconductance $= 0.6A/mm$

- Normally on due to trapped charge; depletion or enhancement mode

- Best $BV_{DS} = 10V - 12V$

#433: SiO₂-based HIGFET

ID normalized

TIME (sec.)
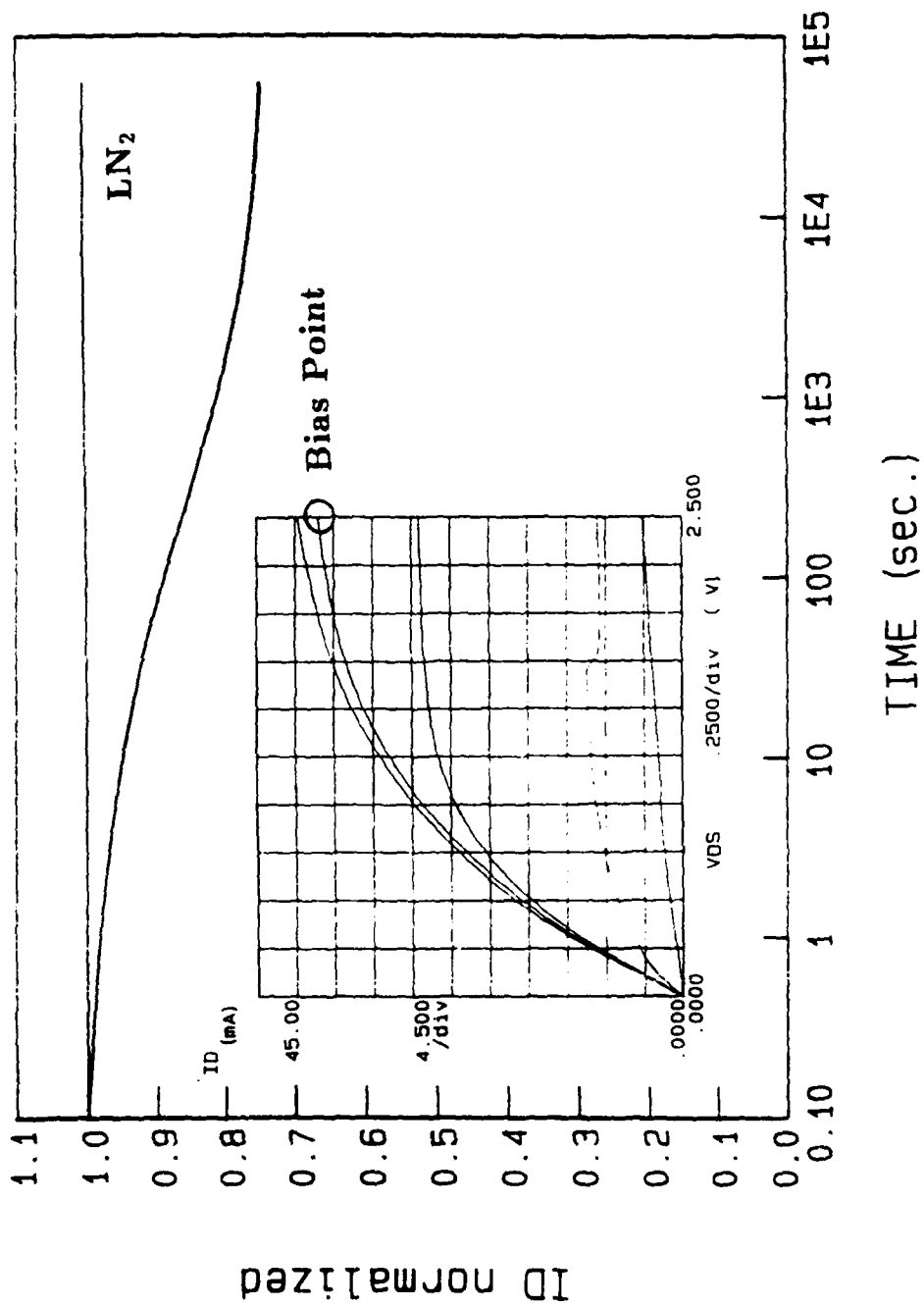
SiO$_2$-Based HIGFET I$_d$ drift at 5GHz

- DC bias V$_D$=2.5V, V$_G$=0V

- 5GHz V$_g$ superposed, 6dB gain

- DC bias at peak transconductance

- Drift $< \pm 4\%$ over 15 Hours
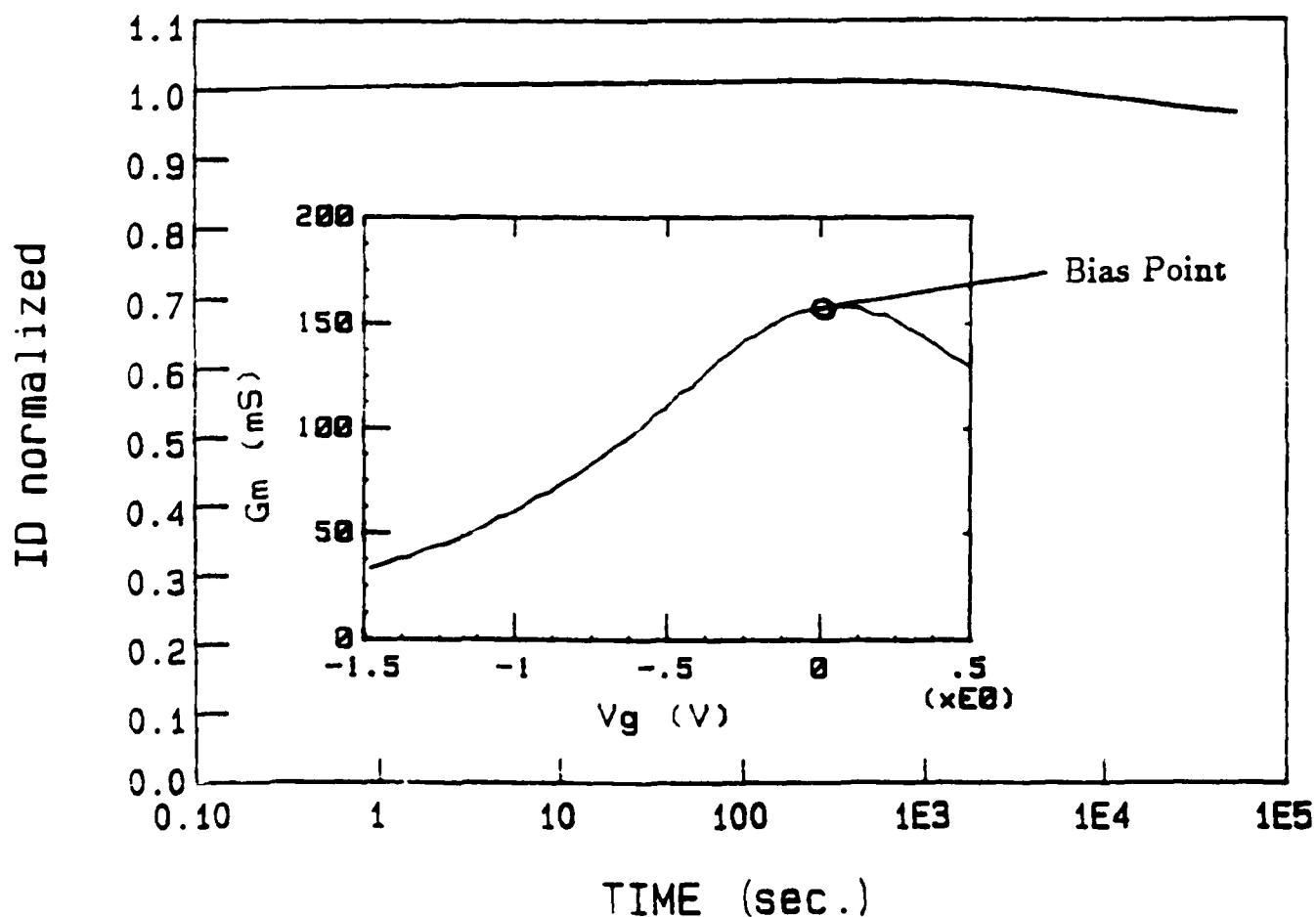
HIGFET Microwave Performance

7–SEP–88 08:42:11

InAlAs-based HIGFET, $L_G=2.5\mu m$

SiO_2-based overlapping-gate HIGFET, $L_G=2.5\mu m$

Gain (dB)

24.0

20.0

16.0

12.0

8.0

4.0

0.0

$5'10^{-1}$ 10^0 10^1 10^2
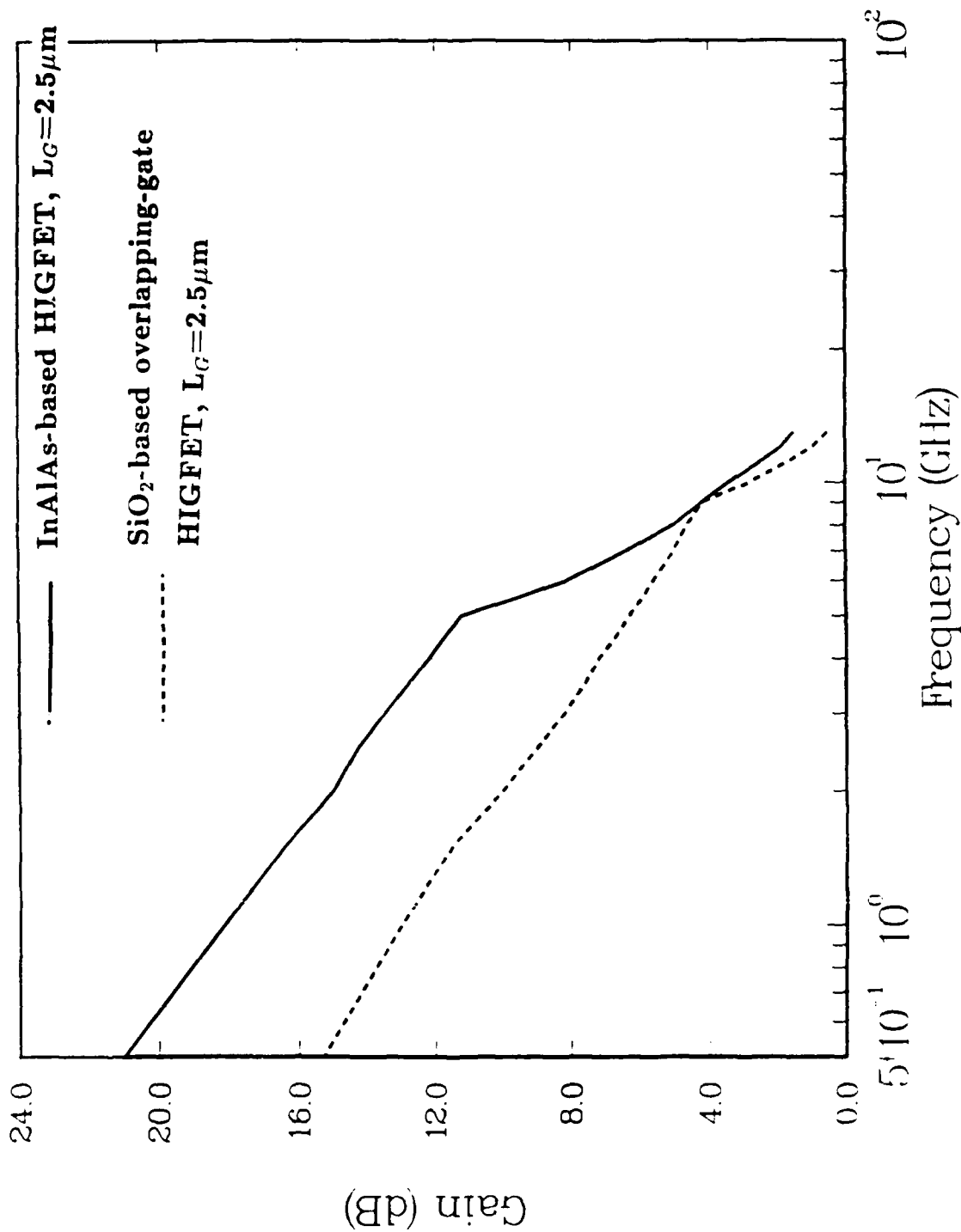
Frequency (GHz)

Summary and Future Work

- SiO_2-Based HIGFET More Promising than InAlAs-Based

- SiO_2-Based HIGFETs Promising Microwave Power Devices

- Need to Process Short Gate-Length Devices for Extended Frequency Performance

- Emphasize High Power Density ($>1\,W/mm$)

- Control of Bulk and Interface Traps for Normally-Off, Enhancement Mode Switching FETs

INTERFACE PROCESSING FOR HIGH PERFORMANCE INSULATED GATE DEVICES ON InP

R. Chang, Z. Zou, K. Han, R. Iyer, and D. L. Lile

Colorado State University
Fort Collins, CO

Fig. 1.

16   14   13   15   17
12 Copper Sulfide
11 Aluminum Oxide
10 Aluminum
20

Fig. 2.

26   25
12 Copper Sulfide
11 Aluminum Oxide
10 Aluminum

Fig. 3.

19   18   17
14   13   12   15
16   11
10
20   21
22
23

Fig. 4.

30   33   32   34   31
11
10

Fig. 5.

35   37   38   36
11
10

Fig. 6.

51   42
44   40
43   47
50   49
48   41
.6   45

Fig. 6ª.

44
56
40
43   58   58
55   55
58   57   57   58
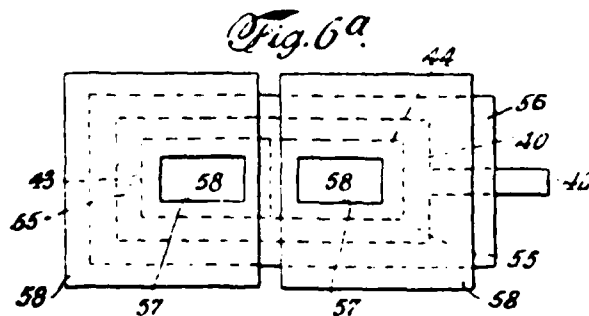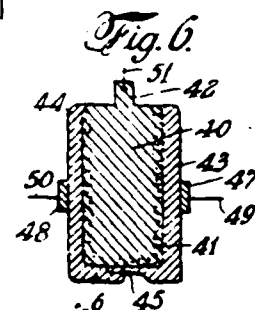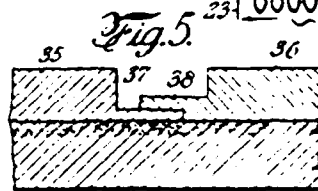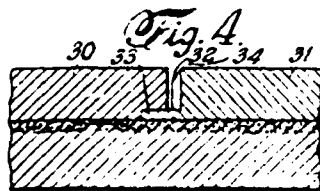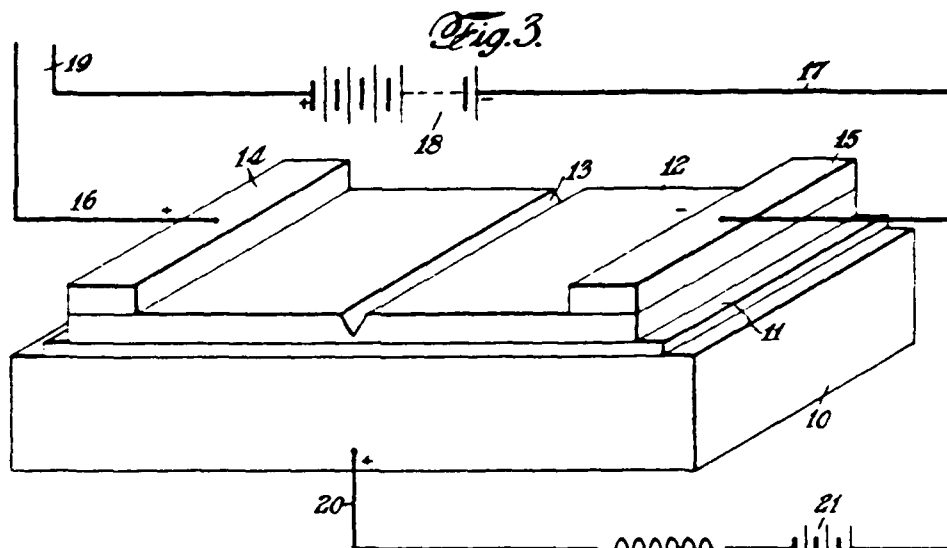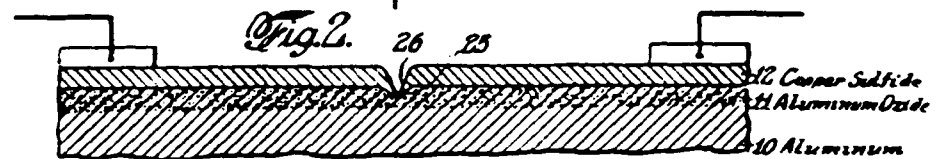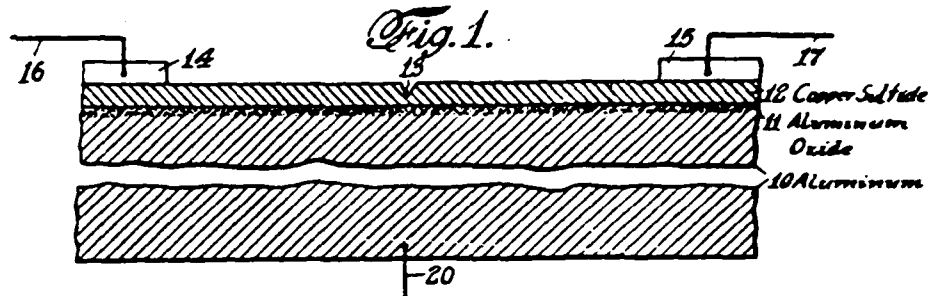
INVENTOR
Julius Edgar Lilienfeld
BY
ATTORNEY

NORMALIZED CHANNEL CURRENT

TIME (sec)

3×10^0

10^0

10^{-1}

10^0 10^1 10^2 10^3 10^4

119 K
148 K
198 K
249 K
296 K

[handwritten:] $\int$ ... ??? (GaAs is worse!)

H. HASEGAWA, T. SAWADA

InP

N_{ss} (cm^{-2} eV^{-1})

Fig 2 A summary of density distributions of interface states in various InP MIS systems The numbers on the curves correspond to the references from which the data were obtained

Types of insulator	Curves
Native oxide	
Anodic oxide	29
Plasma oxide	30
Deposited insulator	
SiO$_2$	31
Al$_2$O$_3$	32
Al$_2$O$_3$, native oxide	37
Langmuir film	38
P$_3$N$_5$	39

GaAs

N_{ss} (cm^{-2} eV^{-1})

Fig 1 A summary of density distributions of interface states in various GaAs MIS systems The numbers on the curves correspond to the references from which the data were obtained

Types of insulator	Curves
Native oxide	
Thermal oxide	7, 8
Anodic oxide*	9 12, 25
Plasma oxide	13, 14
Deposited insulator	
SiO$_2$	15*, 16, 18
Si$_3$N$_4$	9**, 15, 19, 20, 27
Al$_2$O$_3$	15**, 21, 23
Al$_2$O$_3$, native oxide	26
Ge$_3$N$_4$	28
Ga$_x$O$_y$N$_z$	24, 27*
SiO$_2$ Si$_3$N$_4$	15***

MASS SPECTROMETER

PHOTOLUMINESCENCE

PUMP

EXHAUST

GROWTH
CHAMBER

EXCITED
OXYGEN

PLASMA
CHAMBER

PHOSPHOROUS
GENERATOR

P_4 or P_3N_5

OXIDANT
(O_2 or N_2O)

REACTANT (eg. SiH_3 for SiO_2)

GAS
HANDLING

INDIRECT (REMOTE) PLASMA ENHANCED
CVD GROWTH PROCESS FOR LOW
TEMPERATURE DIELECTRICS

SILICON DIOXIDE

PHOSPHOROUS OXIDE/SILICON DIOXIDE

• THEORY

CAPACITANCE (pF)

VOLTAGE (volts)

Table 1

PHOSPHOROUS (or As) TREATMENTS
(CVD dielectric growth except as noted).

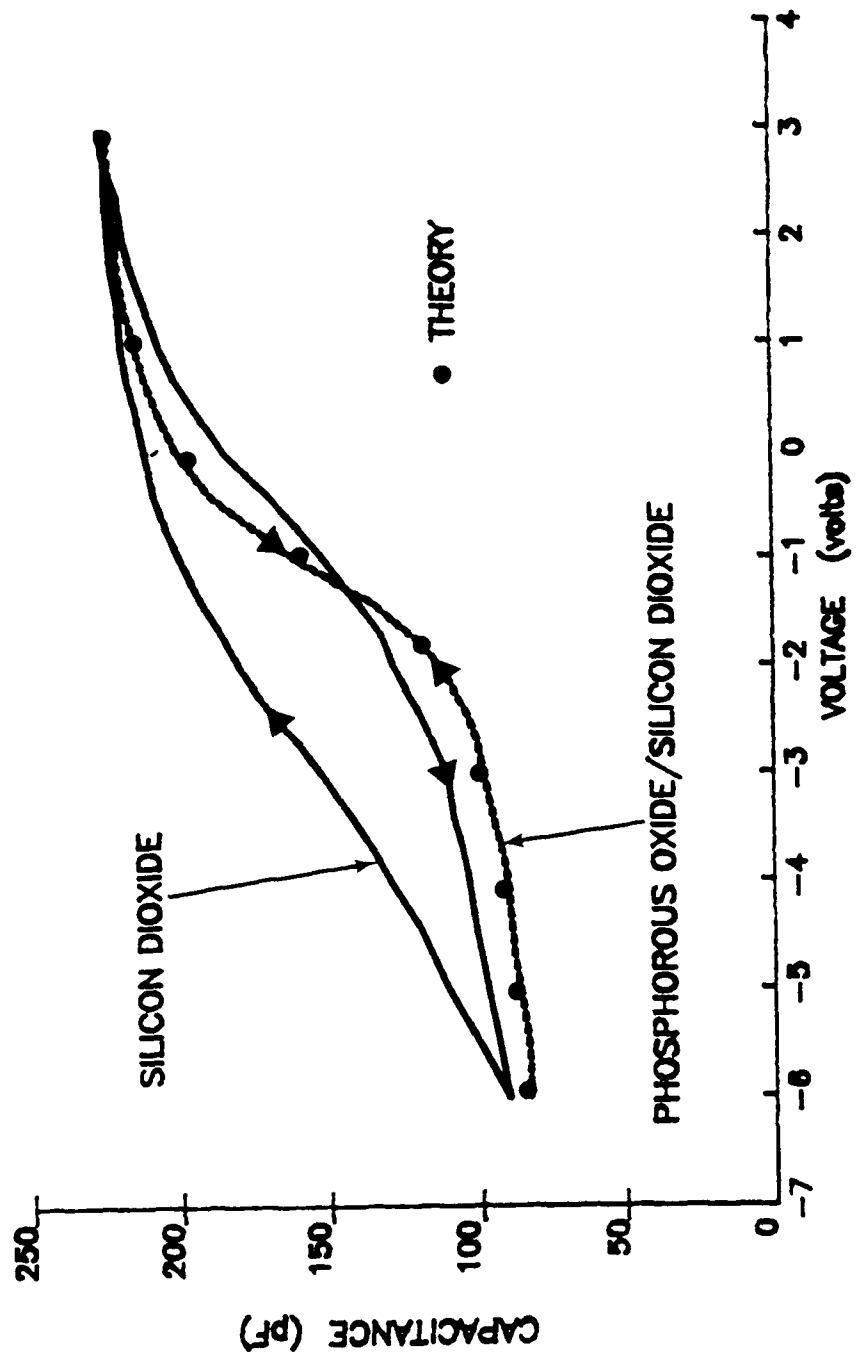| Author	Reference	Dielectric and reactants	Result
Y. Hirota and T. Kobayashi	J. Appl. Phys. $\underline{53}$ 5037 (1982)	Thermal nitride + P_3N_5 from (PH_3 + NH_3)	$N_{ss} \sim 10^{12}$ near CB. PL used to identify a reduction in surface defects due to PH_3
E. Yamaguchi et al.	Thin Solid Films $\underline{103}$, 201 (1983)	PAs_xN_y from ($A_3H_3^y$ + PH_3 + NH_3)	As in addition to P decreases $N_{ss} \sim 10^{11}$
Y. Furukawa	Japan J. Appl. Phys. $\underline{23}$ 1157 (1984)	PN from ($POCL_3$ + NH_3)	Improved C-V
T. Kobayashi et al.	J. Appl. Phys. $\underline{55}$, 3876 (1984)	Al_2O_3 in presence of tri ethyl phosphorous	Order of magnitude reduction in N_{ss} with phosphorous
S. Krawczyk et al.	Electron. Lett. $\underline{20}$, 255 (1984).		As pretreatment inhibits surface degradation during annealing
L. G. Meiners	Thin Solid Films 113, 85 (1984)	AlP_xO_y grown in presence of PH_3	Increased resistivity and lower $N_{ss} \sim 10^{11}$
O. Mikami et al.	Japan J. Appl. Phys. $\underline{23}$ 1408 (1984)	PN from ($POCL_3$ + NH_3)	Inversion MISFET on p-InP with ~zero drift
E. Yamaguchi and M. Minakata	J. Appl. Phys. $\underline{55}$ 3098 (1984)	BN from (NH_3 + B_2H_6) in presence of PH_3	$N_{ss} \sim$ few 10^{10} near mid gap
R. Blanchet et al.	Appl. Phys. Lett. $\underline{46}$, 761 (1985)	e-gun evaporated Al_2O_3 with As pretreatment	Reduced C-V hysteresis and reduced N_{ss} inferred near CB
K. P. Pande and D. Gutierrez	Appl. Phys. Lett. $\underline{46}$, 416 (1985)	SiO_2 from (SiH_4 + N_2O) in presence of P_4	MISFETs on SI InP with drift $< 3\%$ and enhanced $u \sim 3450$. $N_{ss} \sim 8 \times 10^{10}$
R. Schachter et al.	Appl. Phys. Lett. $\underline{47}$, 272 (1985)	Evaporated P_4 - high resistivity semi-conductor	C-V gives $N_{ss} \sim 2 \times 10^{10}$ at minimum and general reduction in N_{ss} near CB

BALTZERS QMA-120
MASS SPECTROMETER

TURBO PUMP

TRIPLE ORIFICE
VALVE

PUMPING
SYSTEM

N_2

DEPOSITION CHAMBER

InP SAMPLE

O_2

SiH_4

FURNACE

RED
PHOSPHOROUS

N_2
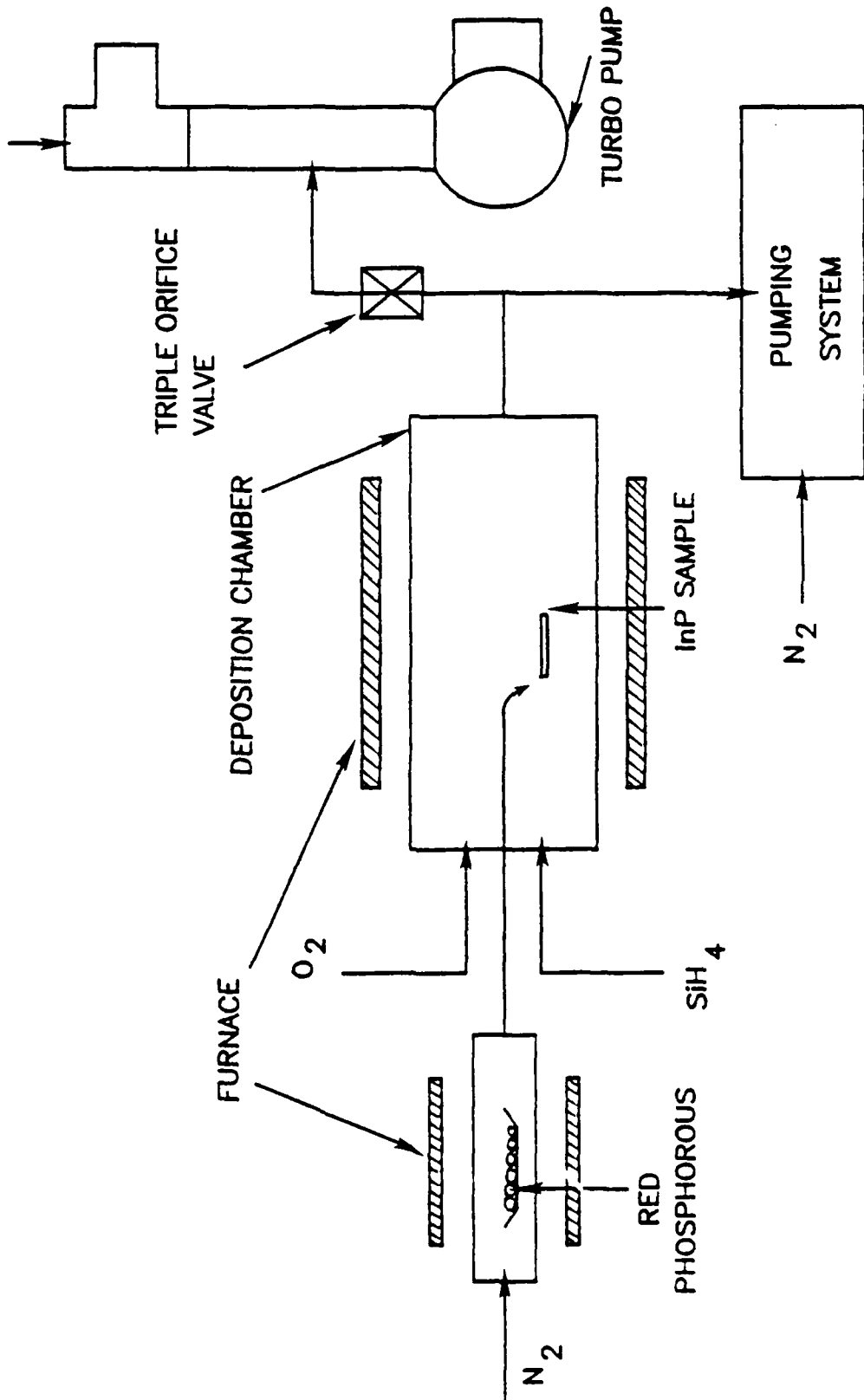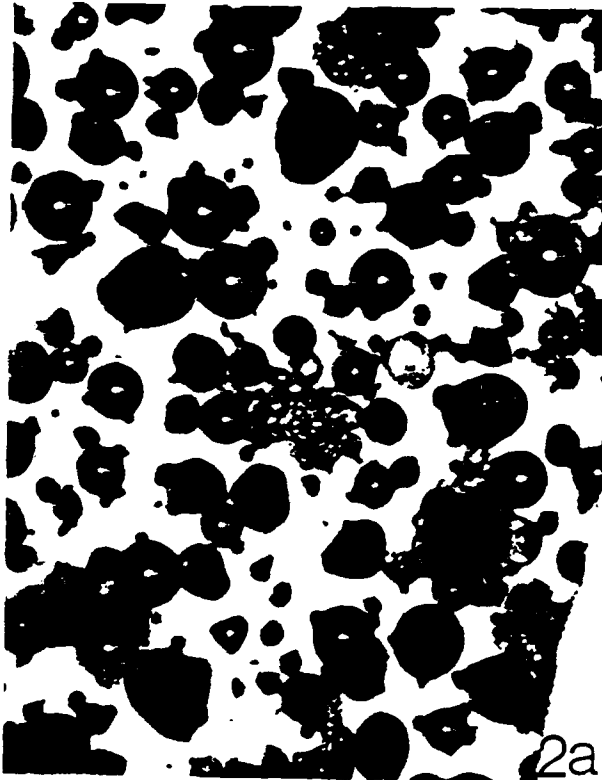
2a
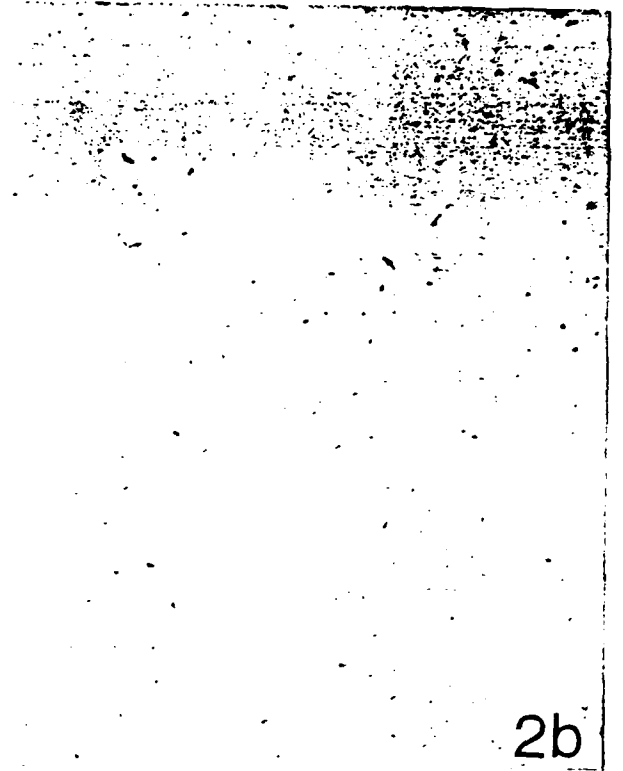
2b
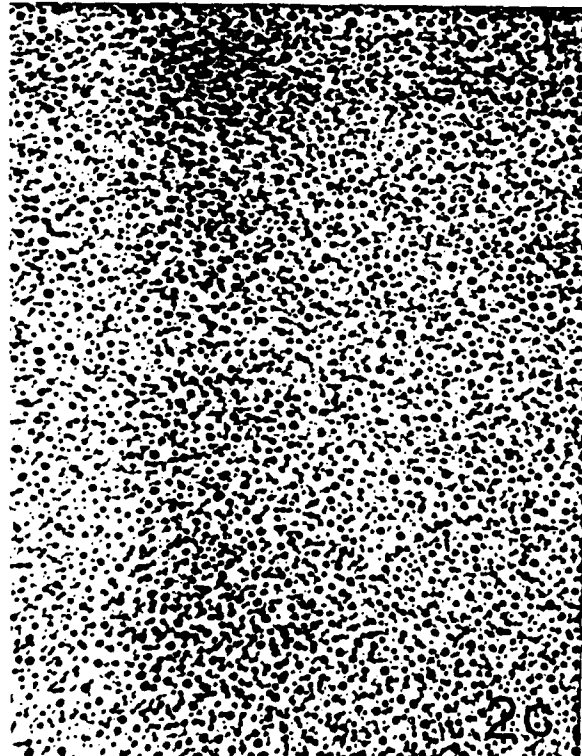
2c

HIGH FREQUENCY (1MHz) AND QUASI–STATIC C–V

DATA FOR SULFURIZED InP.

* WITH IPCVD SiO$_2$ AS DIELECTRIC
* HIGH FREQUENCY C–V EXHIBITS A CLOCKWISE
  HYSTERESIS OF 200mV.
* SWEEP RATE : 100mV/Sec FOR HIGH FREQENCY
              : 64mV/Sec FOR QUASI–STATIC C–V

THEORY

EXPERIMENT

CAPACITANCE (pf)

VOLTAGE (volts)
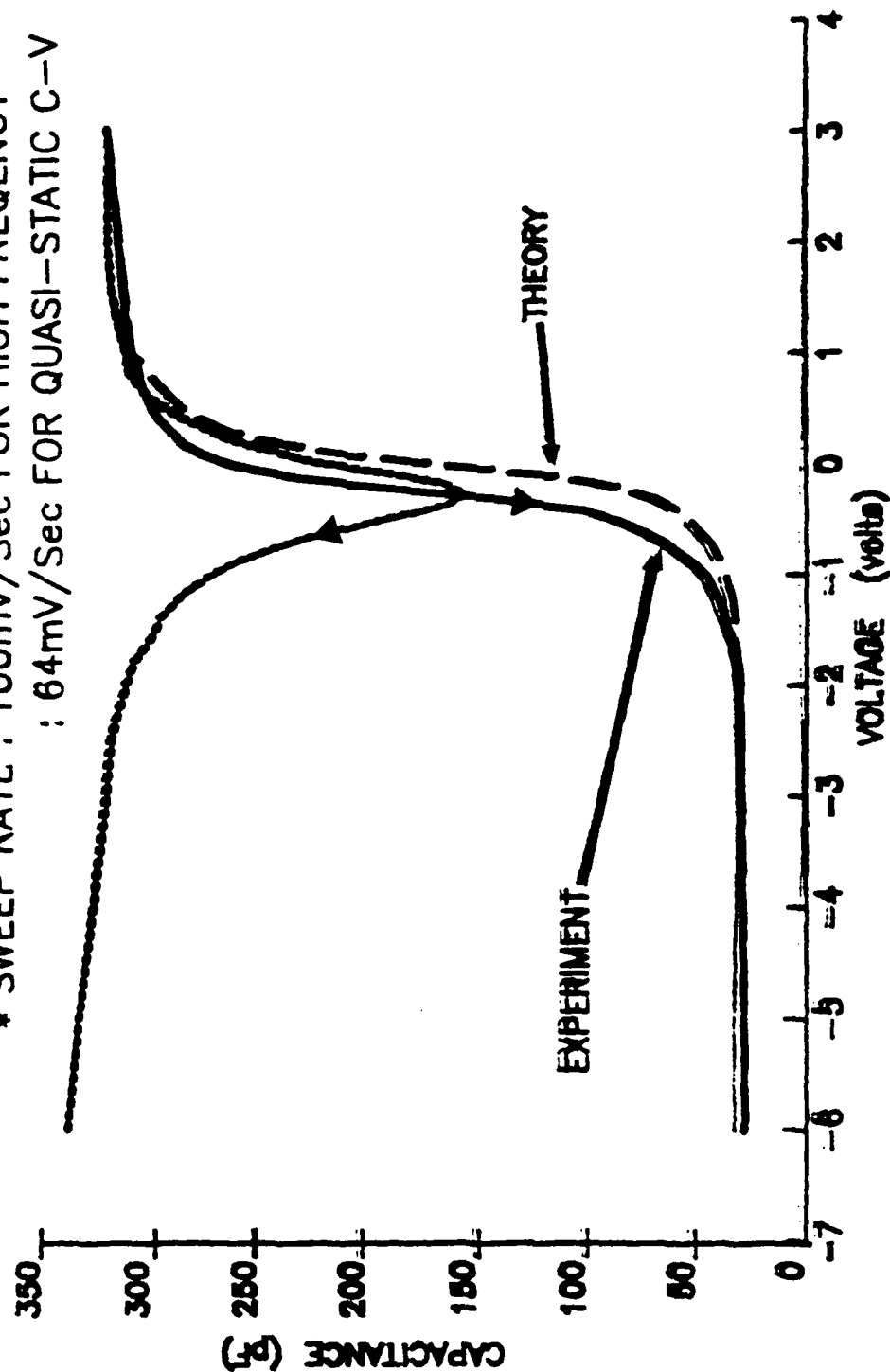
SURFACE STATE DENSITY OF SULFURIZED

n-TYPE InP

BERGLUND ANALYSIS

TERMAN ANALYSIS

N_{ss} $(cm^2 \cdot ev)^{-1}$

1.E+14
1.E+13
1.E+12
1.E+11
1.E+10
1.E+9

-1.2   -1   -.8   -.6   -.4   -.2   0   .2

SURFACE POTENTIAL (ev)

a)

SINGLE DONOR

TRIPLE ACCEPTOR

b)

$$V_P^+ + 4e^- \rightleftharpoons V_{In}^- \, In_P^{--}$$

$$\Rightarrow \frac{[V_{In} \, In_P]}{[V_P]} = \frac{N_A}{N_D} = K n^4$$
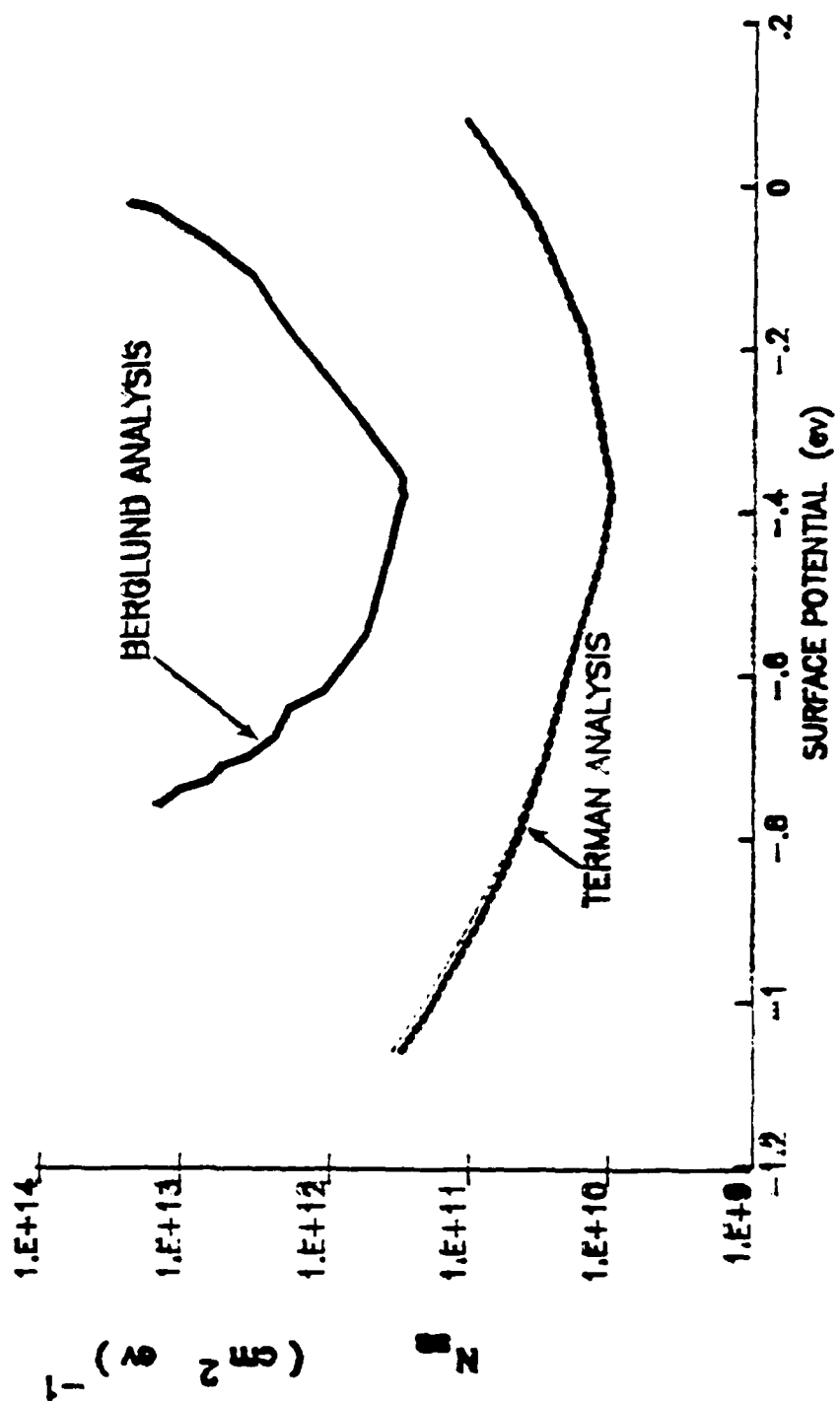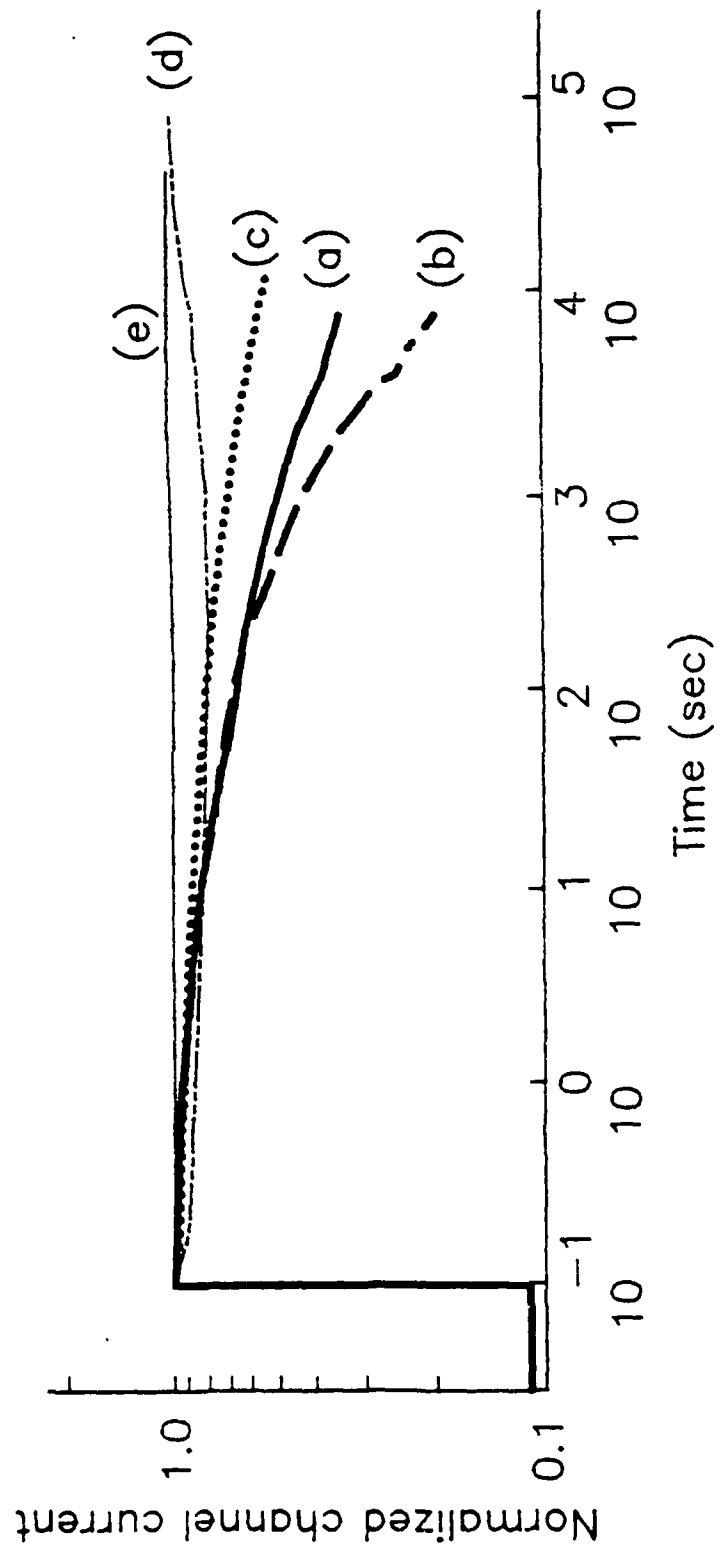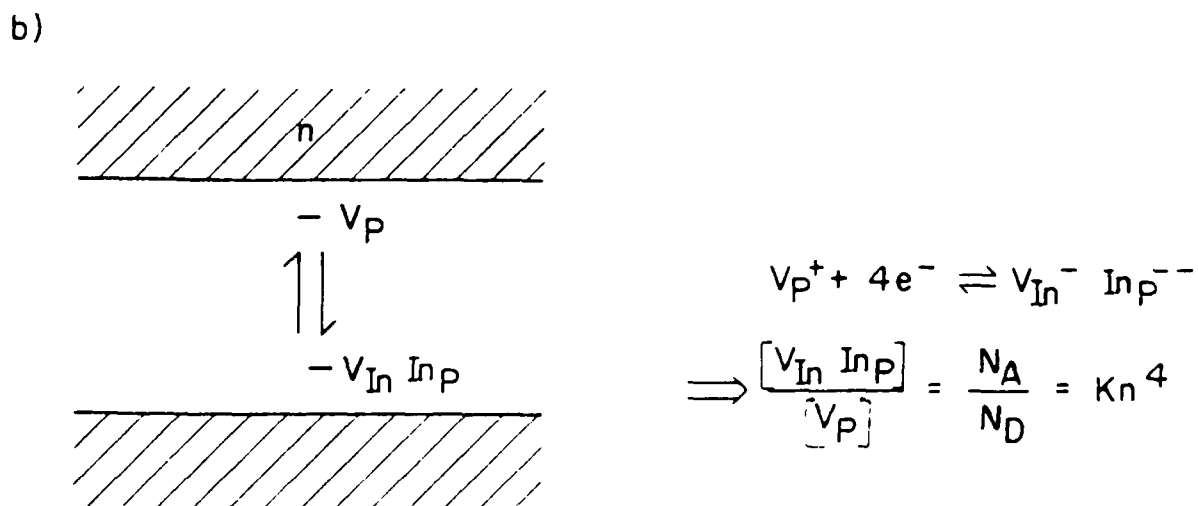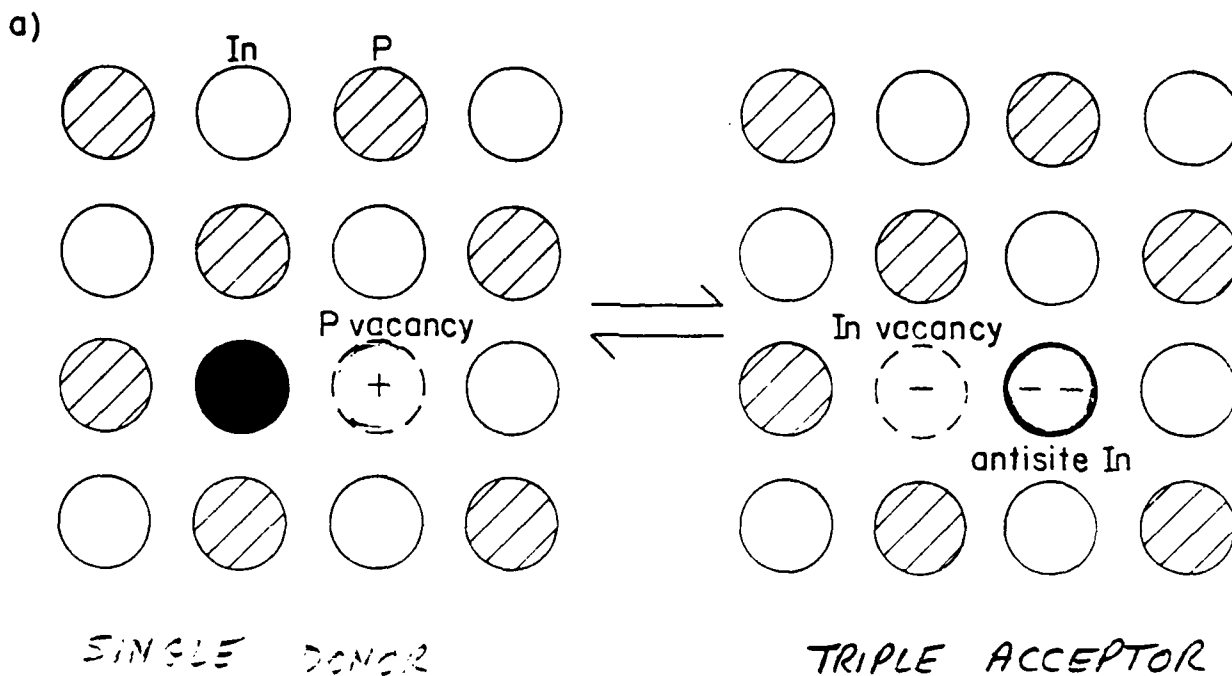
VAN VECHTEN AND WAGER

MULTI-CHANNEL InGaAs MESFETS HAVING UNIFORM DC AND MICROWAVE GAINS

A. Fathimulla, H. Hier, J. Abrahams, and E. Hempfling

Allied-Signal Aerospace Company
Aerospace Technology Center
9140 Old Annapolis Road
Columbia, MD 21045

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9140 OLD ANNAPOLIS ROAD
COLUMBIA, MD 21045

Allied-Signal Aerospace Company

AlliedSignal

n+ - InGaAs/UNDOPED InAlAs MESFETs (MISFETs)

- HEAVILY DOPED CHANNEL

- DOPING IN NARROW BAND GAP MATERIAL

- HIGHER BREAKDOWN VOLTAGE

- DESIGN FLEXIBILITY OF THE STRUCTURE

- MULTI-CHANNEL DEVICE

InGaAs (cap)

undoped InAlAs

n⁺- InGaAs

undoped InGaAs

InAlAs (Buffer)

SI - InP

STRUCTURE OF A SINGLE-CHANNEL n^+- InGaAs/UNDOPED InAlAs MESFET

InGaAs (cap)

undoped InAlAs

n - InGaAs

undoped InAlAs

n⁺ - InGaAs

undoped InAlAs

n⁻ - InGaAs

undoped InAlAs

n⁺ - InGaAs

InAlAs (Buffer)

SI - InP

STRUCTURE OF A MULTI-CHANNEL n⁺- InGaAs/UNDOPED InAlAs MESFET

MESA ISOLATION

OHMIC CONTACT

GATE
DEPOSITION

OVERLAY

GATE
ISOLATION

GATE LENGTH: 0.5μm

SOURCE-DRAIN: 4.0μm
DISTANCE

OHMIC CONTACT: AuGe-Ni

GATE METAL: Ti-Pt-Au

PROCESS SEQUENCE OF THE MESFET
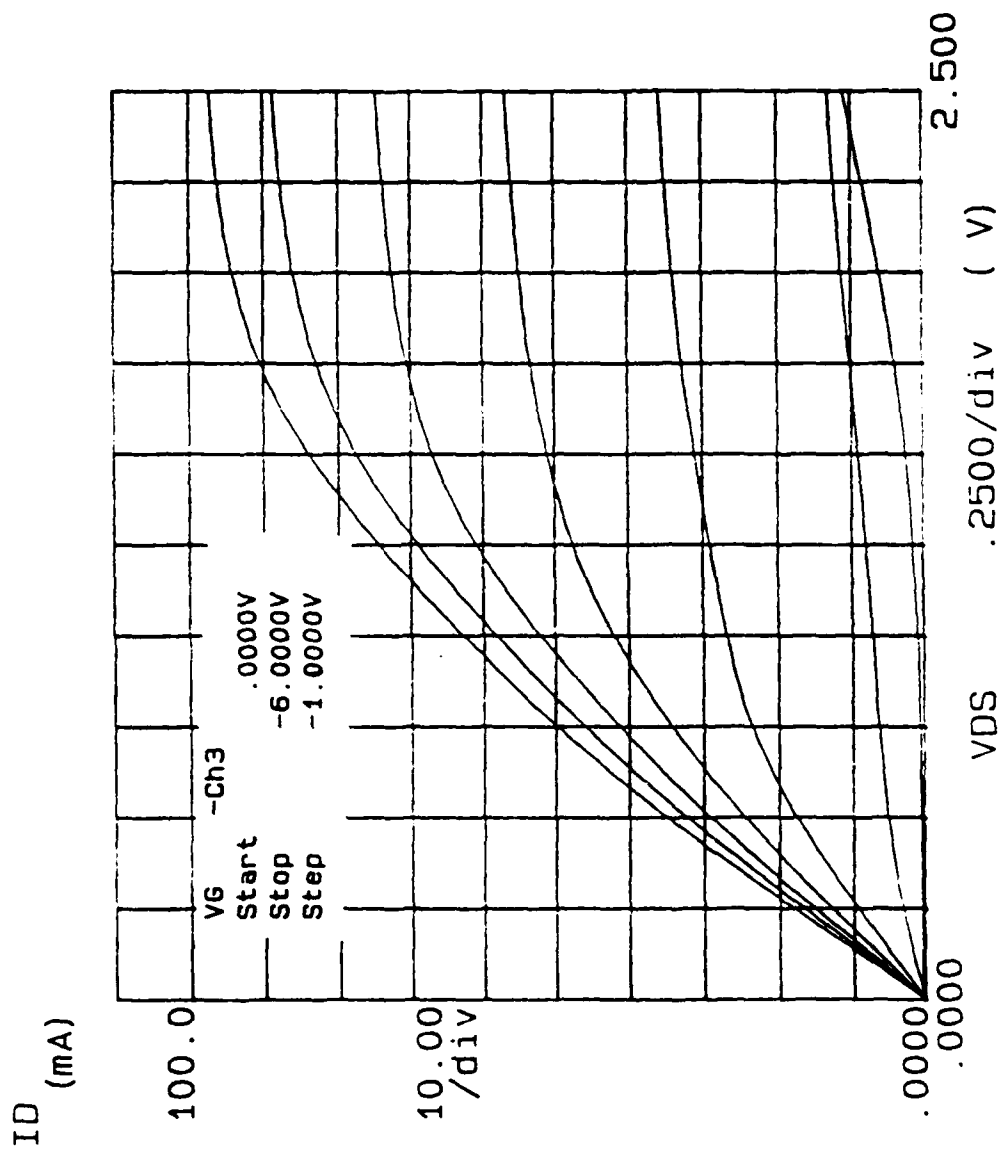
IV-CHARACTERISTICS OF THE SINGLE-CHANNEL
n⁺- InGaAs/InAlAs MESFET

ID (mA)

100.0

10.00 /div

.0000

VG   -Ch3
Start   .0000V
Stop   -6.0000V
Step   -1.0000V

.0000   VDS   .2500/div   (V)   2.500

GM (S)

MARKER (-4.8800V , .235E-03)

	VG	-Ch3	
	Linear sweep		
	Start		.0000V
	Stop		-6.0000V
	Step		- .0800V

240.0
E-03

24.00
/div

.0000
-6.000

VG   .6000/div   (V)   .0000

TRANSCONDUCTANCE VS GATE VOLTAGE OF THE
SINGLE-CHANNEL n⁺- InGaAs/InAlAs MESFET
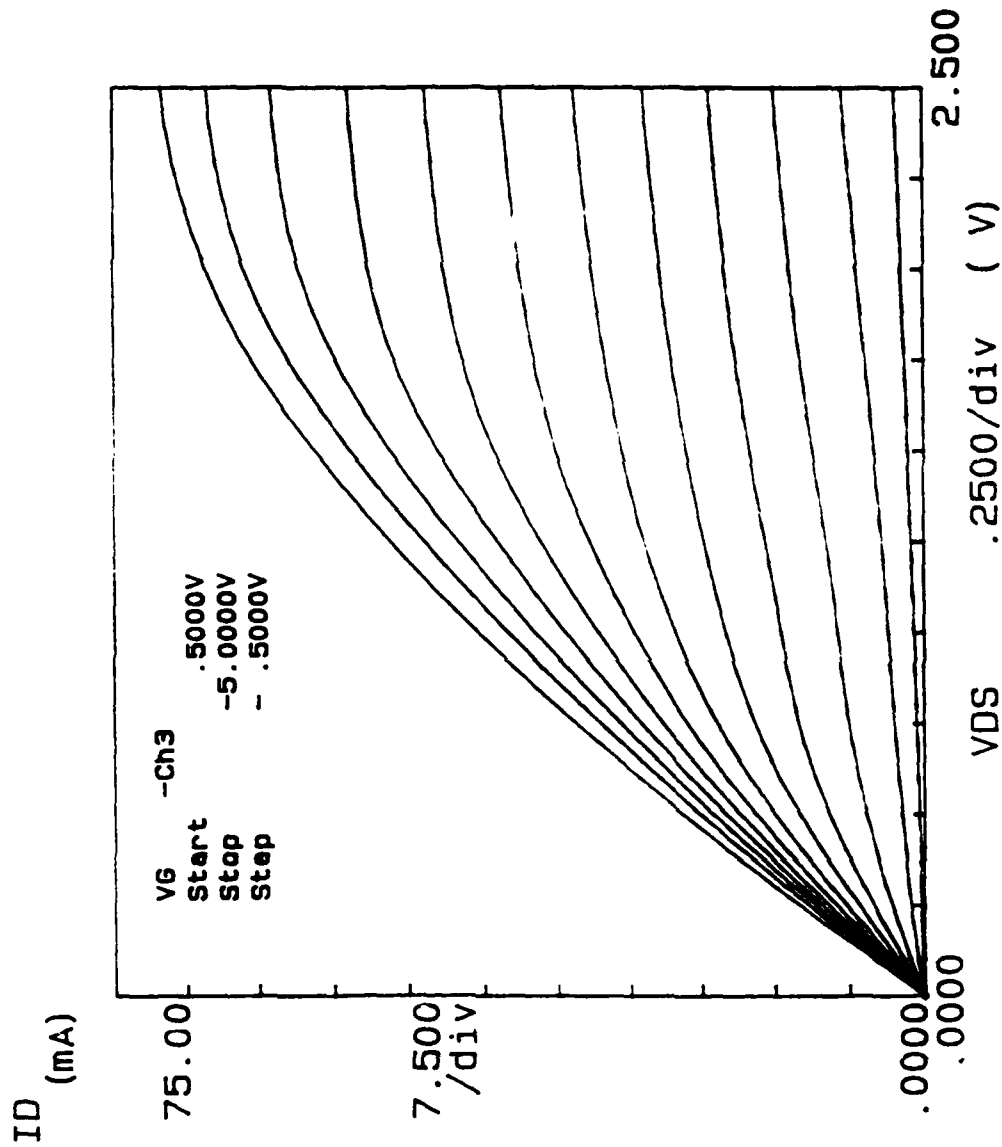
AlliedSignal

IV-CHARACTERISTICS OF THE MULTI-CHANNEL
n⁺- InGaAs/InAlAs MESFET

ID (mA)

VDS   .2500/div   (V)

VG   -Ch3
Start   .5000V
Stop   -5.0000V
Step   - .5000V

75.00

7.500
/div

.0000

.0000

2.500
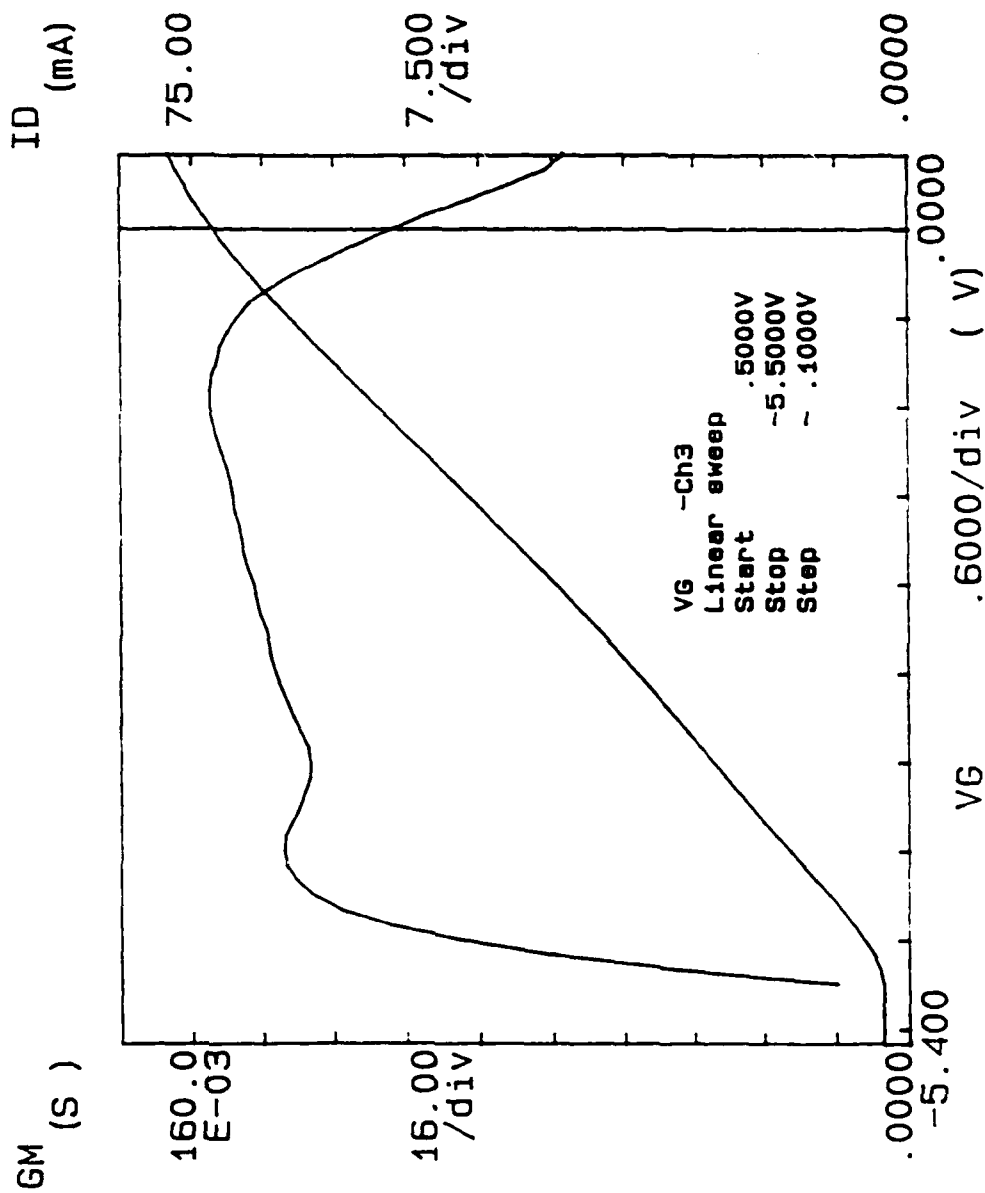
TRANSCONDUCTANCE VS GATE VOLTAGE OF THE
MULTI-CHANNEL n⁺- InGaAs/InAlAs MESFET

IV-CHARACTERISTICS OF THE MULTI-CHANNEL
n^+-InGaAs/InAlAs MESFET

(a) IV

(b) g_m

DRAIN CURRENT (mA)

SOURCE-DRAIN VOLTAGE (volts)

$V_g = 0$
$V_g = -0.5$

TRANSCONDUCTANCE (mS/mm)

GATE BIAS (volts)
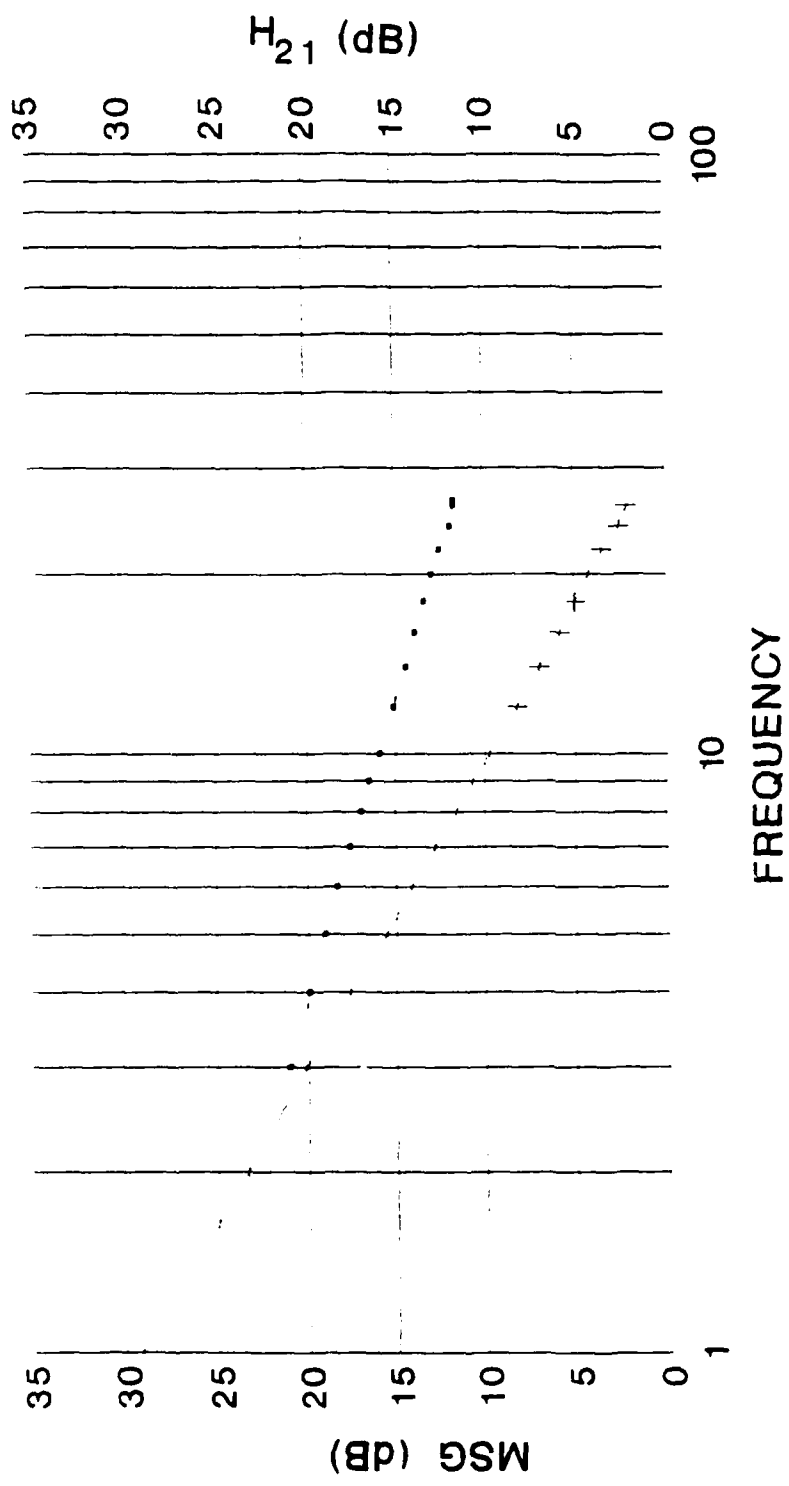
AlliedSignal

MSG AND H_{21} VS FREQUENCY OF THE SINGLE-CHANNEL MESFET
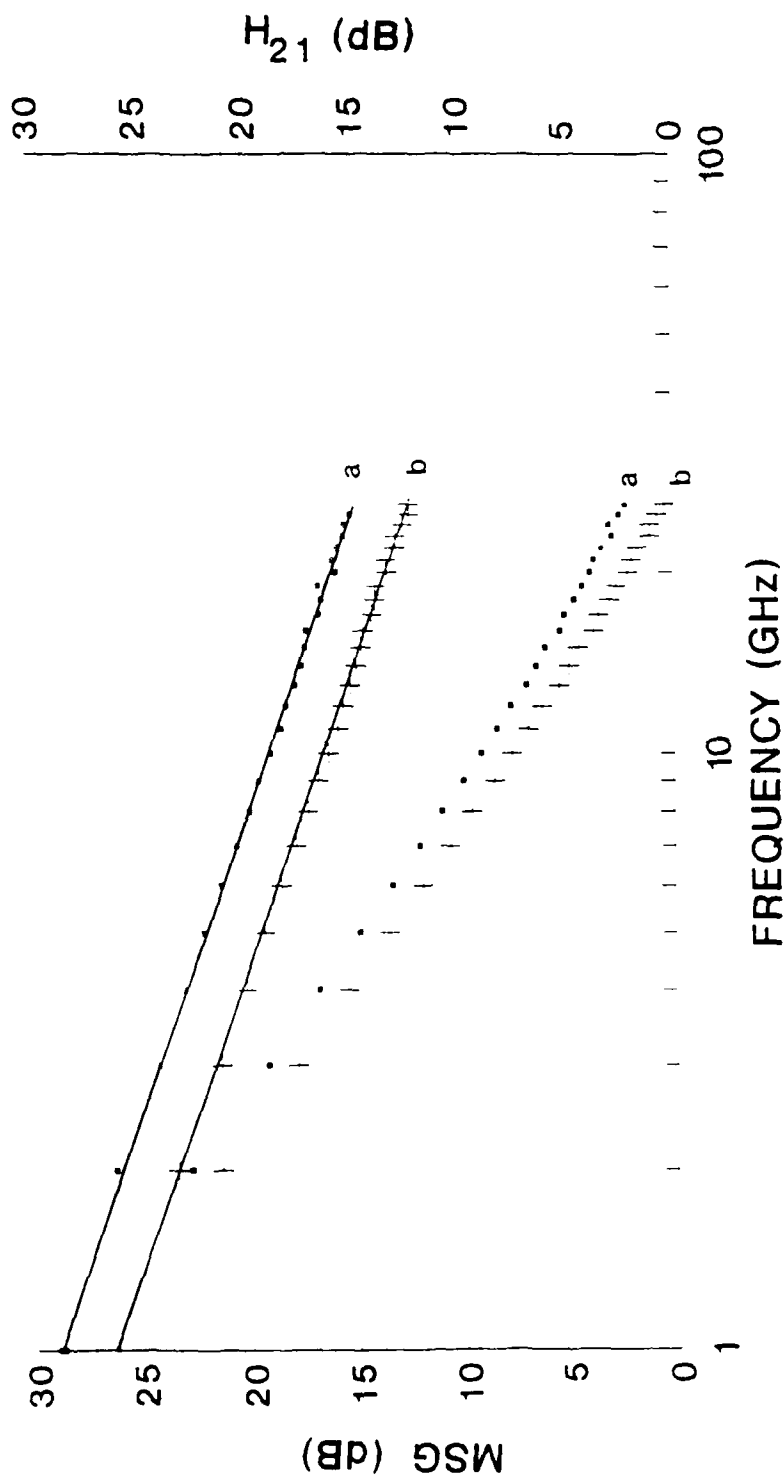
MSG AND H$_{21}$ VS FREQUENCY OF THE MULTI-CHANNEL MESFET
a) 200 μm, b) 100 μm

Allied-Signal Aerospace Company

AlliedSignal

306
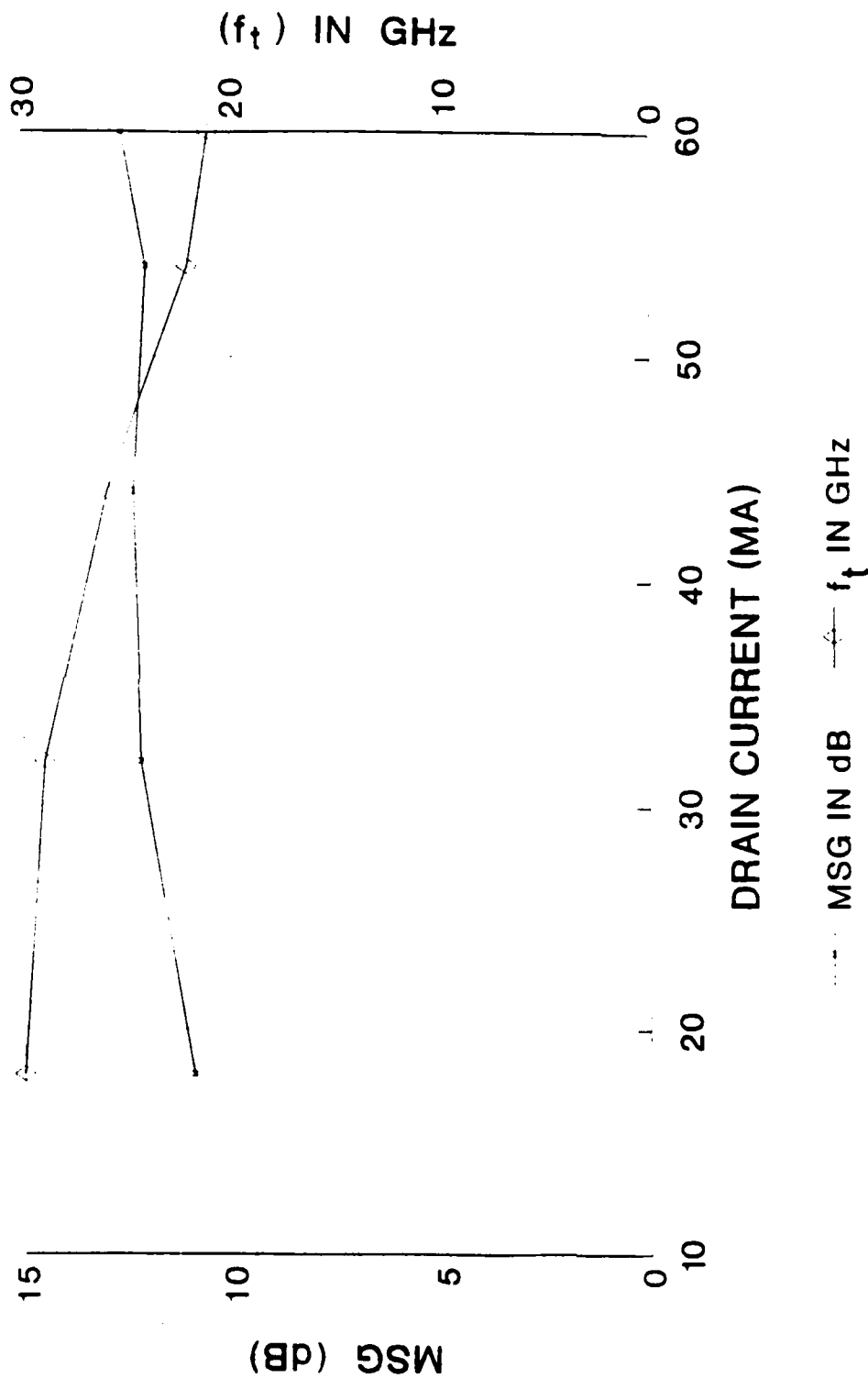
MSG AND f_t VS DRAIN CURRENT OF THE MULTI-CHANNEL MESFET
AT 26.5 GHz

Allied-Signal Aerospace Company

GAIN VERSUS Vds FOR MULTI-CHANNEL
InGaAs/InAlAs MESFET
AT 26.5 GHz

MSG (dB)

SOURCE-DRAIN VOLTAGE
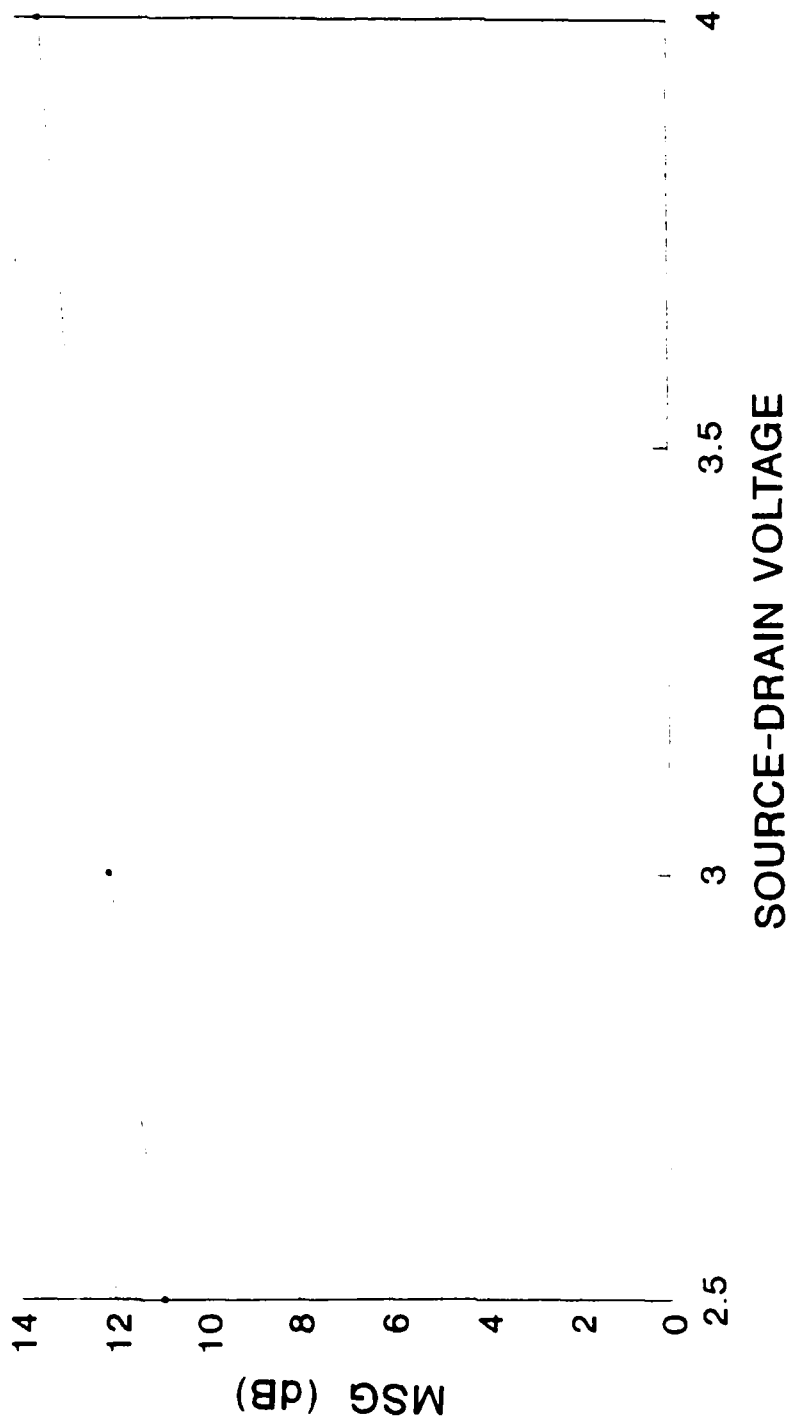
DC AND MICROWAVE PERFORMANCE OF InGaAs MESFETs

DEVICE STRUCTURE	DRAIN CURRENT (A/mm)	TRANS-CONDUCTANCE (mS/mm)	MSG (dB) @ 26.5 GHz	f_t * (GHz)
SINGLE CHANNEL	.6	275	14.0 dB	29
SINGLE CHANNEL	1	245	11.0 dB	31
MULTI-CHANNEL	0.8	152±8 (-0.5 TO -5.0V)	11.8 ± 0.7	21-31

Allied-Signal Aerospace Company

Allied Signal

309

InP JUNCTION FETS WITH A NITRIDE-REGISTERED GATE METALLIZATION

J. B. Boos, W. Kruppa* and B. Molnar

U. S. Naval Research Laboratory
Washington, DC 20375

*George Mason University
Fairfax, VA 22030

InP JUNCTION FETS WITH A

NITRIDE-REGISTERED GATE METALLIZATION

J. B. BOOS, W. KRUPPA*, B. MOLNAR

U. S. NAVAL RESEARCH LABORATORY

WASHINGTON D. C. 20375

* GEORGE MASON UNIVERSITY
FAIRFAX, VIRGINIA 22030

PLANAR, FULLY ION-IMPLANTED InP JFET DEVELOPMENTS

1) NITRIDE-REGISTERED GATE METALLIZATION

2) Be/P CO-IMPLANTATION

3) ADDITION OF Ni IN P-TYPE GATE METALLIZATION

InP JFET APPLICATIONS

1. POWER FET

2. InP-BASED OPTOELECTRONICS

3. MILLIMETER WAVE MONOLITHIC CIRCUITS

FULLY ION-IMPLANTED InP JFET
FABRICATION APPROACHES

PREVIOUS APPROACH:
ETCH-BACK PROCESS
TO DEFINE GATE LENGTH
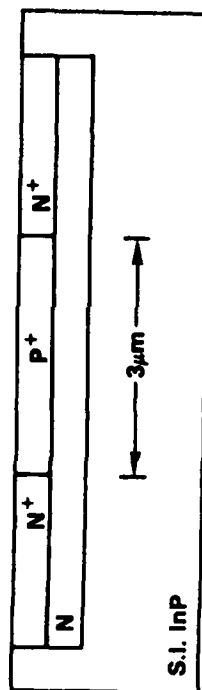
NEW APPROACH:
NITRIDE-REGISTERED GATE METAL
SIMPLIFIES GATE LENGTH DEFINITION

316
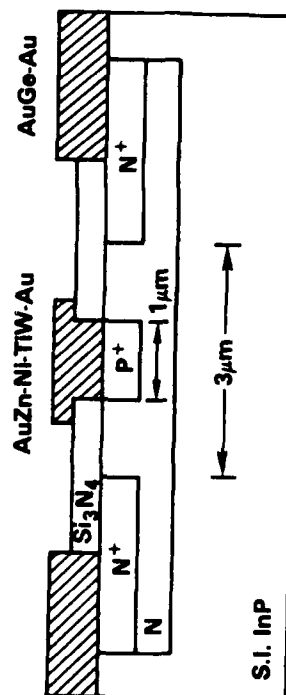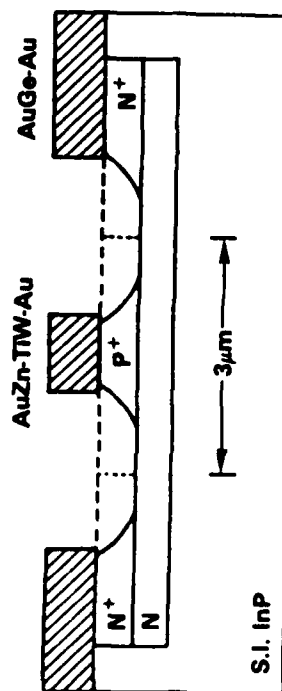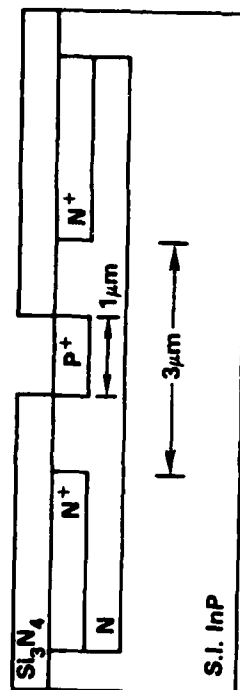
ION-IMPLANTED P-N JUNCTION LSS DISTRIBUTIONS

WITH Be/P CO-IMPLANTATION

^{31}P: 200 keV, 9×10^{13}cm^{-2}
110 keV, 2×10^{13}cm^{-2}

WITH Be IMPLANTATION ONLY

^{28}Si: 500 keV, 1×10^{13}cm^{-2}
^{9}Be: 55 keV, 9×10^{13}cm^{-2}
       30 keV, 2×10^{13}cm^{-2}

NRL

317

AuZn/Ni/TiW/Au
InP JFET GATE METALLIZATION

1 μm

400Å TiW
150Å Ni

2500Å Au

100Å Au
500Å AuZn

P$^+$ InP — 4000Å

N InP — 3000Å

S.I. InP
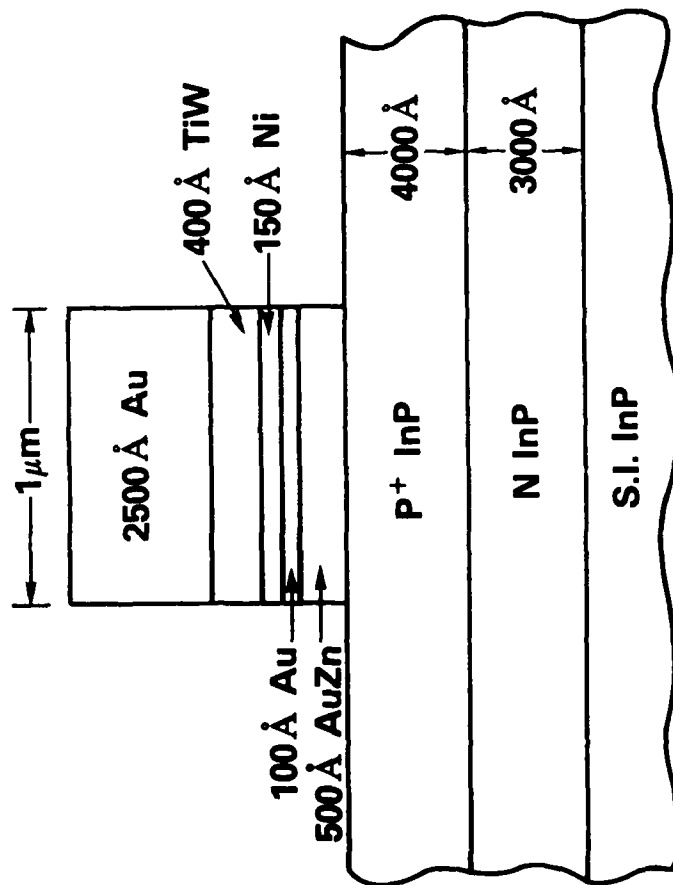
	WITHOUT Ni	WITH Ni
CONTACT ADHESION	MODERATE	EXCELLENT
SPECIFIC CONTACT RESISTANCE ($\Omega \cdot cm^2$)	$\sim 4 \times 10^{-5}$	$\sim 2 \times 10^{-5}$

NRL

ION-IMPLANTED P-N JUNCTION DIODE CHARACTERISTICS
(GATE AREA = 1μm × 150μm)
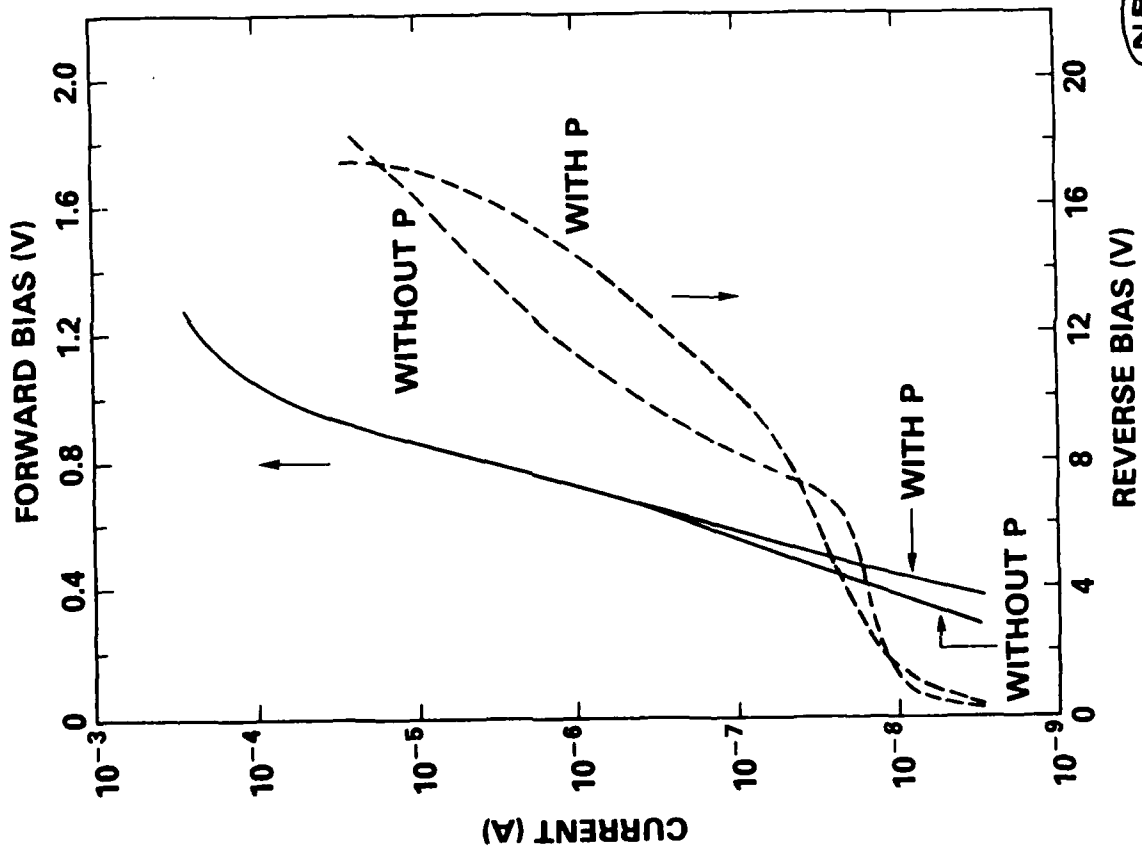
FULLY ION-IMPLANTED InP JFET CHARACTERISTICS

(GATE WIDTH=150μm, GATE LENGTH≈1μm)

$V_{GS}=0$ TO $-14V$
WITH 2V STEP
$g_m=10ms$ PER DIV.

WITH Be/P CO-IMPLANTATION

$V_{GS}=0$ TO $-5V$ WITH 1V STEP
$g_m=5ms$ PER DIV.

WITH Be IMPLANTATION ONLY

NRL

320
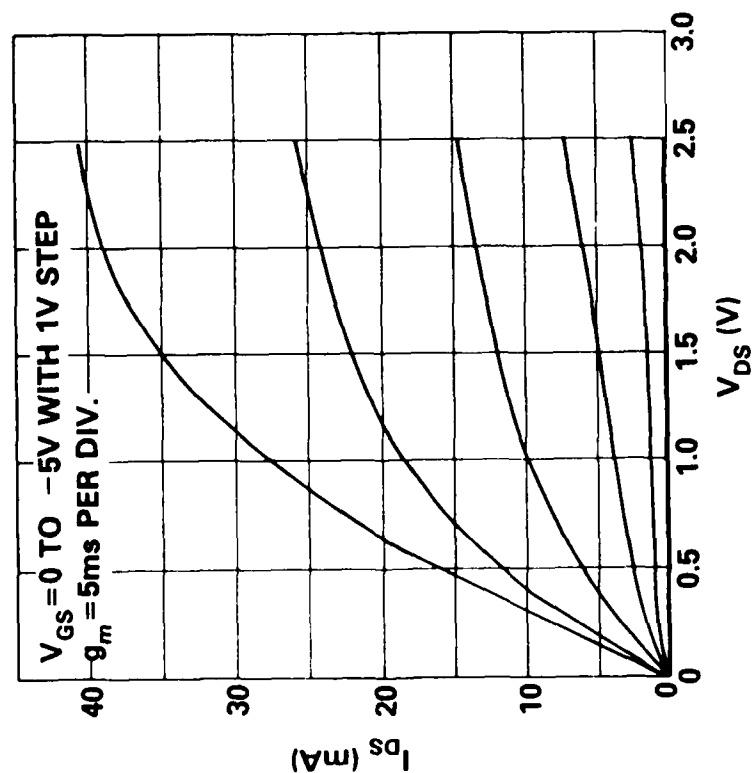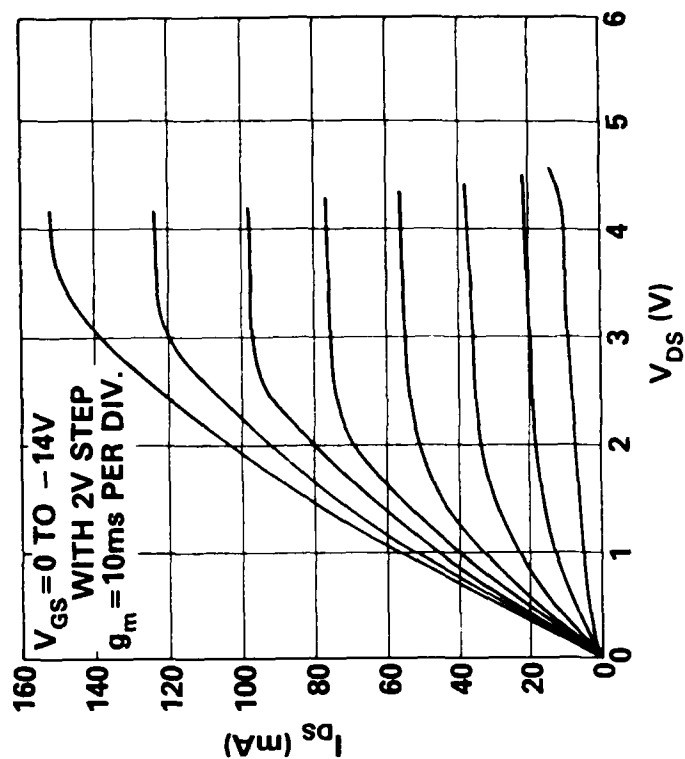
InP JFET SUMMARY

1. Demonstrated highest transconductance (140 mS/mm) InP JFET with a new nitride-registered gate process. Process may be suitable for sub-micron gate lengths.

2. Demonstrated use of P/Be co-implantation with proximity rapid thermal annealing which significantly reduced Be-redistribution.

3. Developed new p-type InP gate ohmic contact with improved adhesion and the lowest contact resistance reported.

InP-BASED PSEUDOMORPHIC HIGH-SPEED DEVICES REALIZED BY MOLECULAR BEAM EPITAXY

Pallab K. Bhattacharya

Solid State Electronics Laboratory and
Center for High Frequency Microelectronics
Department of Electrical Engineering and Computer Science
The University of Michigan
Ann Arbor, MI 48109-2122

InP-Based Pseudomorphic High-Speed Devices Realized by Molecular Beam Epitaxy

Pallab K. Bhattacharya

Solid State Electronics Laboratory and
Center for High Frequency Microelectronics
Department of Electrical Engineering & Computer Science
The University of Michigan, Ann Arbor, MI 48109-2122

Outline

- Background – InP based devices

- Role of Strain in altering the bandstructure and transport properties in thin layers

- Pseudomorphic n- and p-type modulation doped heterostructures

    - Materials properties

    - Device characteristics

- Pseudomorphic Resonant Tunneling Diodes

- Role of Tensile Strain

I.   Background – InP based Devices

Favorable Attributes

- $In_{0.53}Ga_{0.47}As/InP$ with $E_g = 0.74$ eV is useful for fiber-optic communication

- The ternary material also has high μm. high v_E and large Γ - L separation

- $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ heterostructure has high band offset and better carrier confinement

Applications

- High Speed Devices → MODFETs (no D-X related problems)

- Detectors. modulators and lasers

Recent Results

1 μm gate MODFETs

$g_m(ext) \sim 400$ mS/mm

$f_T = 32 - 36$ Ghz

0.1 μm gate MODFETs

$g_m(ext) = 1080$ mS/mm

$f_T = 170$ GHz

N.F. = 0.8 dB

gain = 8.7 dB at 63 GHz

II. Bandstructure and Transport Properties in Pseudomorphic Layers

Effects of Biaxial Strain

- Changes in Bandgap

- Changes in band offsets, resulting in better confinement

- Changes in conduction band effective mass

※ - Changes in valence band structure *and hole masses*

Calculated Electron Effective Masses (Jaffe & Singh)
(Jaffe & Singh)

x	$In_xGa_{1-x}As$			$In_{0.53+x}Ga_{0.47-x}As$		
	$m^*_{unstrained}$	$m^*_{\parallel strained}$	$m^*_{\perp strained}$	$m^*_{unstrained}$	$m^*_{\parallel strained}$	$m^*_{\perp strained}$
0.00	0.066	0.066	0.066	0.045	0.045	0.045
0.05	0.064	0.065	0.064	0.044	0.044	0.045
0.10	0.062	0.064	0.063	0.042	0.043	0.045
0.15	0.060	0.063	0.063	0.040	0.041	0.044
0.20	0.058	0.062	0.062	0.037	0.039	0.044
0.25	0.056	0.061	0.061	0.035	0.037	0.044
0.30	0.054	0.060	0.061	0.033	0.035	0.043
0.35	0.052	0.058	0.060	0.031	0.033	0.043
0.40	0.050	0.057	0.060	0.028	0.030	0.043

Properties of 2-DEG in Pseudomorphic Systems
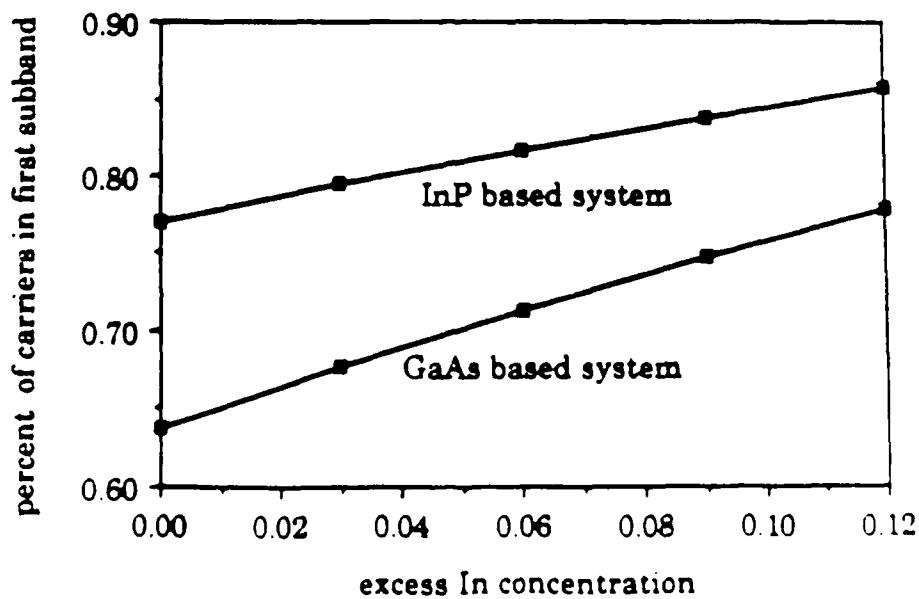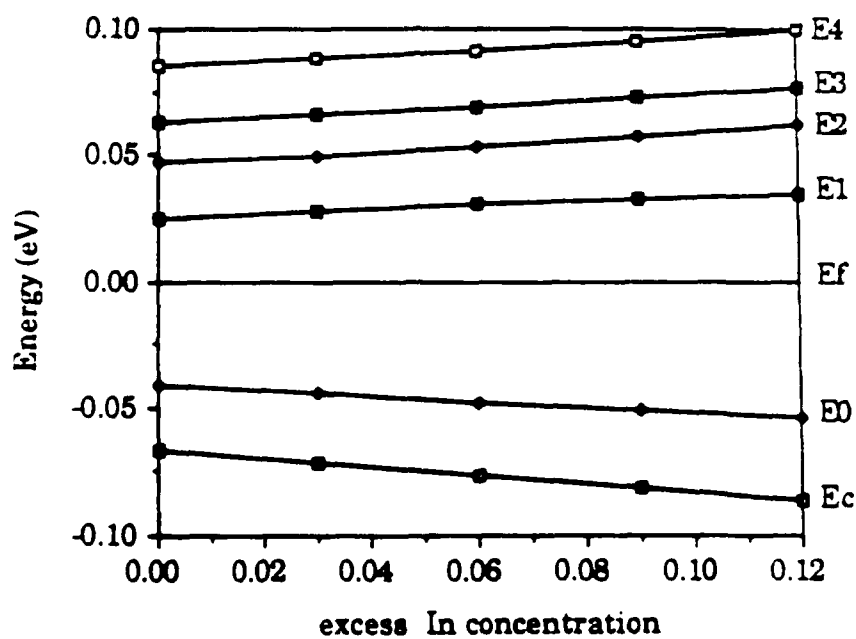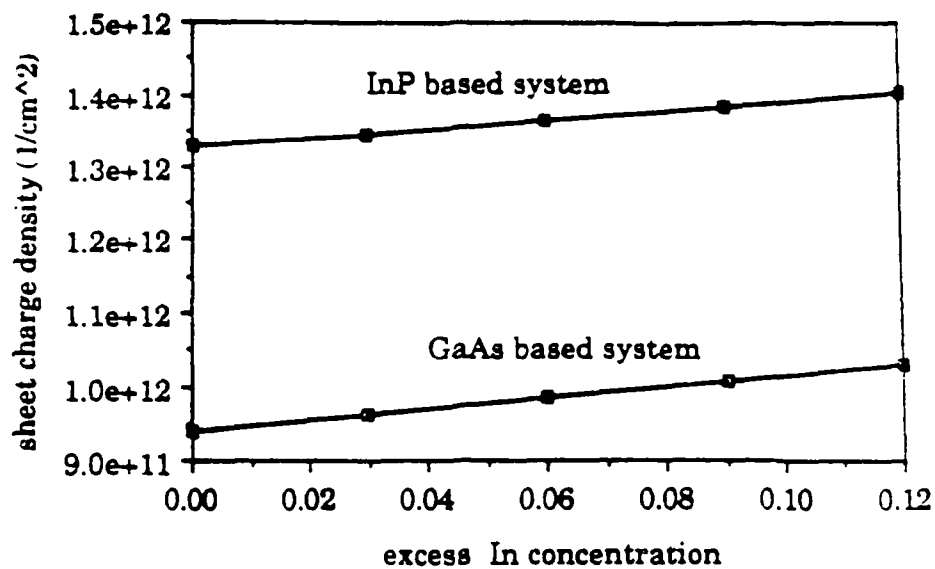
Calculated Hole Effective Masses in Pseudomorphic p-MODFET

[Jaffe, Sekiguchi and Singh, APL, December 1987]

Temp. (K)	subband No.	GaAs channel				In$_{0.12}$Ga$_{0.88}$As channel			
		n, 10^{11}	m^*_{dos}	$E_n - E_f$ (meV)	state	n, 10^{11}	m^*_{dos}	$E_n - E_f$ (meV)	state
300	0	1.19	0.601	−84.8	HH0	1.49	0.257	−56.4	HH0
	1	0.95	0.481	−84.8	HH0	1.15	0.199	−56.4	HH0
	2	0.70	0.686	−102.0	LH0	0.86	0.342	−78.6	HH1
	3	0.64	0.624	−102.0	LH0	0.79	0.313	−78.6	HH1
	4	0.45	0.485	−105.0	HH1	0.53	0.561	−104.0	HH2
	5	0.43	0.463	−105.0	HH1	0.39	0.406	−104.0	HH2
	6	0.35	0.566	−116.0	HH2	0.27	0.569	−122.0	LH0
	7	0.33	0.544	−116.0	HH2	0.19	0.404	−122.0	LH0
	Total	5.06	0.564			5.67	0.324		
77	0	2.28	0.569	−7.22	HH0	2.39	0.144	5.58	HH0
	1	1.24	0.309	−7.22	HH0	1.84	0.111	5.58	HH0
	2	0.61	0.887	−19.7	LH0	0.47	0.267	−13.3	HH1
	3	0.46	0.664	−19.7	LH0	0.41	0.238	−13.3	HH1
	4	0.25	0.399	−20.4	HH1	0.02	0.557	−38.9	HH2
	5	0.21	0.333	−20.4	HH1	0.01	0.383	−38.9	HH2
	6	0.12	0.495	−26.5	HH2	0.00	0.715	−53.7	LH0
	7	0.09	0.375	−26.5	HH2	0.00	0.210	−53.7	LH0
	Total	5.27	0.578			5.15	0.154		

Valence Bandstructure of Pseudomorphic
$In_{0.12}Ga_{0.88}As/AlGaAs$ p-MODFET (Jaffe & Singh)
(Jaffe & Singh)
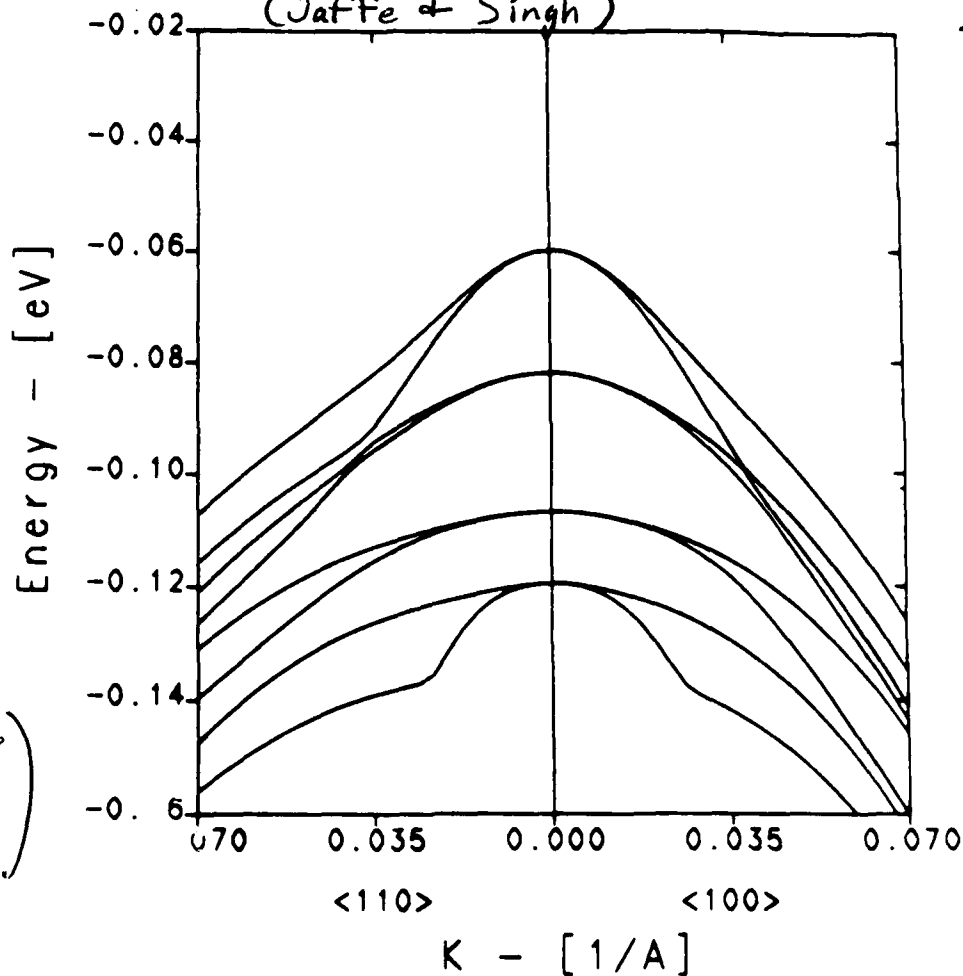
$\left(\mathbf{J}_affe \atop \& \atop Singh \right)$
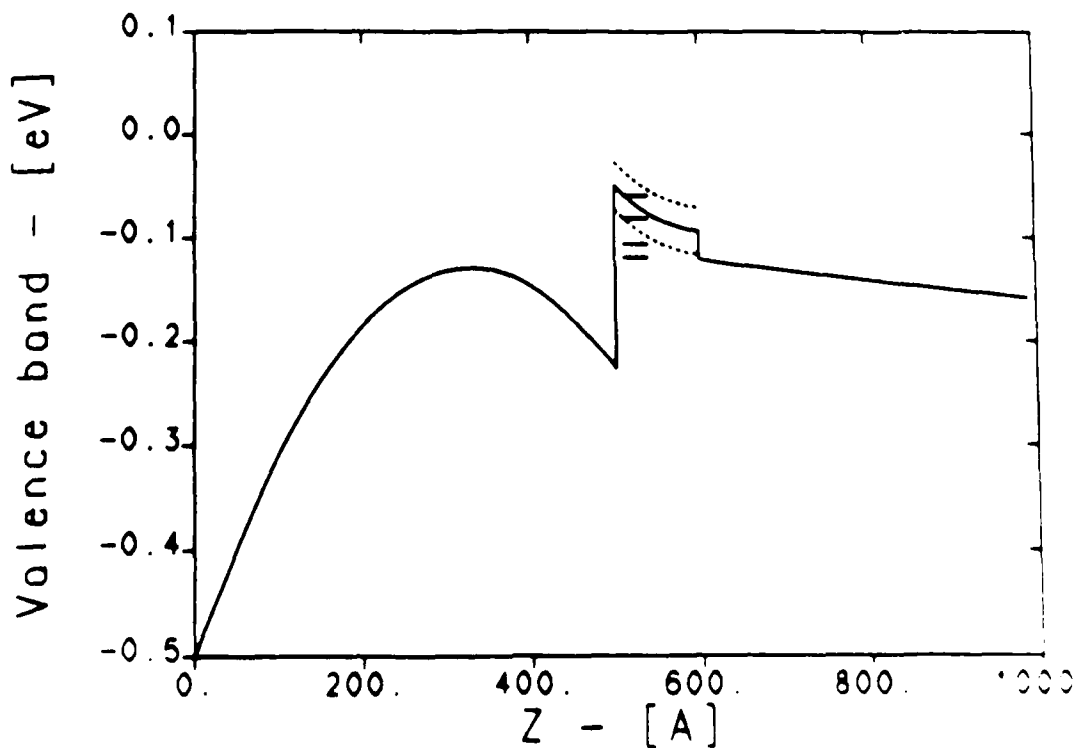
Measured Effective Masses in Pseudomorphic p-MODFETs

100 Å Be GaAs 2×10^18
0.1 μ Be Al_0.15 Ga_0.85 As 2×10^17
150 Å i - Al_0.15 Ga_0.85 As
150 Å i - In_x Ga_1-x As
150 Å i - Al_0.15 Ga_0.85 As
0.1 μ Be Al_0.15 Ga_0.85 As 2×10^17
0.1 μ i - Al_0.15 Ga_0.85 As
0.1 μ i - GaAs

30 period
GaAs (20 Å)/Al_0.15 Ga_0.85 As (20 Å)
superlattice

SI GaAs

Channel inidium composition
Average hole effective mass
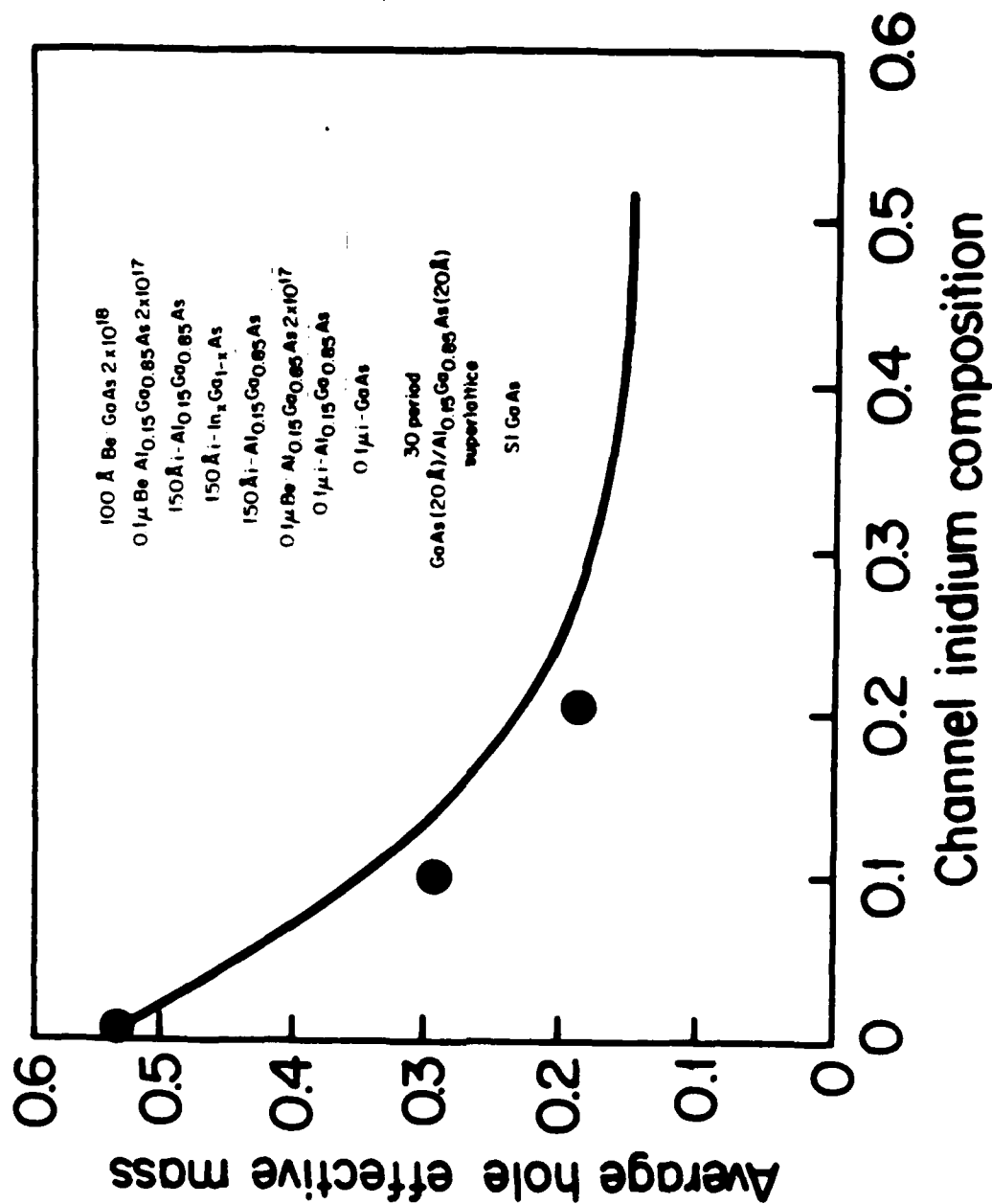
III.   Growth and Characterization of Strained
Heterostructures and Multiquantum Wells

Growth of Near-Perfect InGaAs/InAlAs Modulation-Doped Heterostructures

- Roughness of InAlAs Growth Front:

    - Growth Interruption
    - RHEED Monitoring
    - Recovery with and without InGaAs coverage
    - Control of arrival rate of atoms

- Reduction of impurity movement during growth of inverted structures

    - low temperature InAlAs buffers
      and appropriate growth interruption

Thermodynamic Equilibrium Considerations for Pseudomorphic Growth
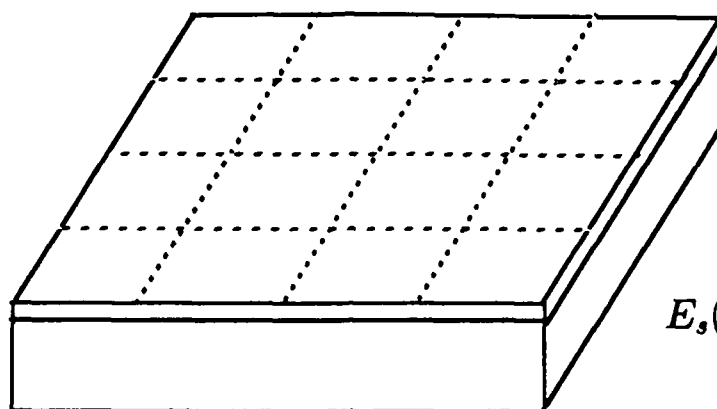
$$E_s(L_d) \sim 4\frac{L_d \cdot W_1}{d_c/R_0}$$

(a) System growing in layer-by-layer growth mode
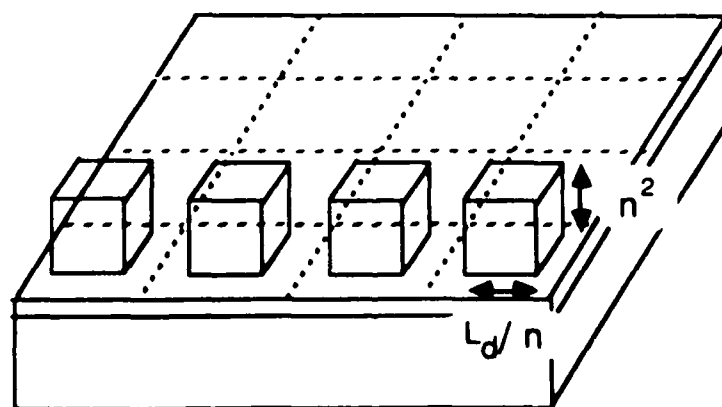
$$E_{sub} \sim 4\frac{L_d \cdot W_1}{n^2 d_c/R_0}$$

$$E_{chem} \cong n^2 \cdot 4\frac{L_d}{n}W_2$$

(b) System growing in 3-D mode with unfulfilled 2nd nearest neighbor bonds

For $d_c < 20$ monolayers $\implies$ Growth is 3-Dimensional

II. Growth Modes

- Lattice-Matched Systems

  Free energy minimum for growth automatically favors smooth surface

- Strained Systems

  Energy minimization favors 3-D growth

IV. Properties of InGaAs/InAlAs Pseudomorphic Heterostructures and Devices

Pseudomorphic $In_x Ga_{1-x}As$ / $In_{0.52} Al_{0.48}As$ ...

n	InGaAs	3 E18	200A
i	InAlAs		300A
n	InAlAs	3E18	200A
i	InAlAs		100A
i	In(x)Ga(1-x)As		150A
i	InGaAs		400A
i	InAlAs		4000A
i	InAlAs/InGaAs		S.L.
S.I.	InP	(100)	

x = 0.53 (Sample A)

x = 0.60 (Sample B)

x = 0.65 (Sample C)
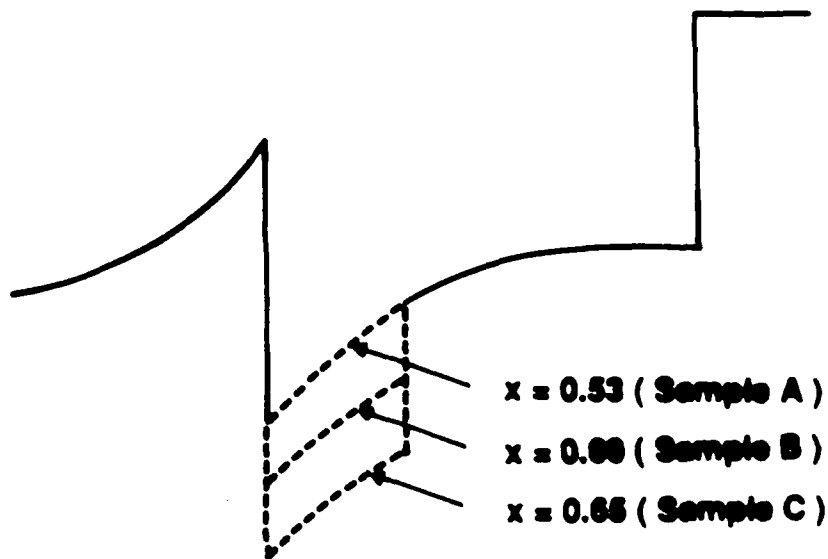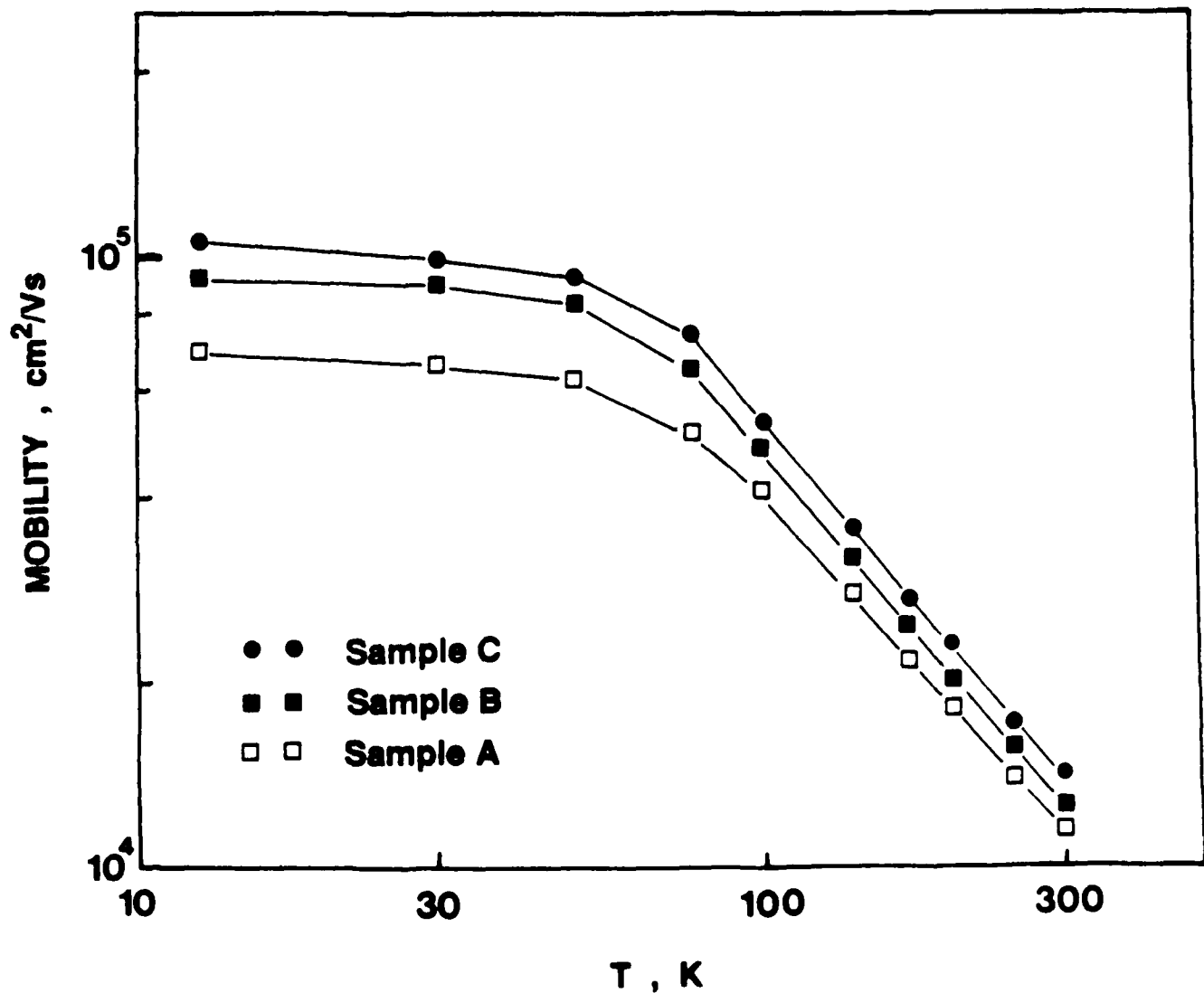
Increased ΔE_c :

→ slightly higher n_{2DEG}

→ lower remote impurity scattering

Increased confinement in first subband :

→ lower intersubband scattering.

10% lower alloy scattering.
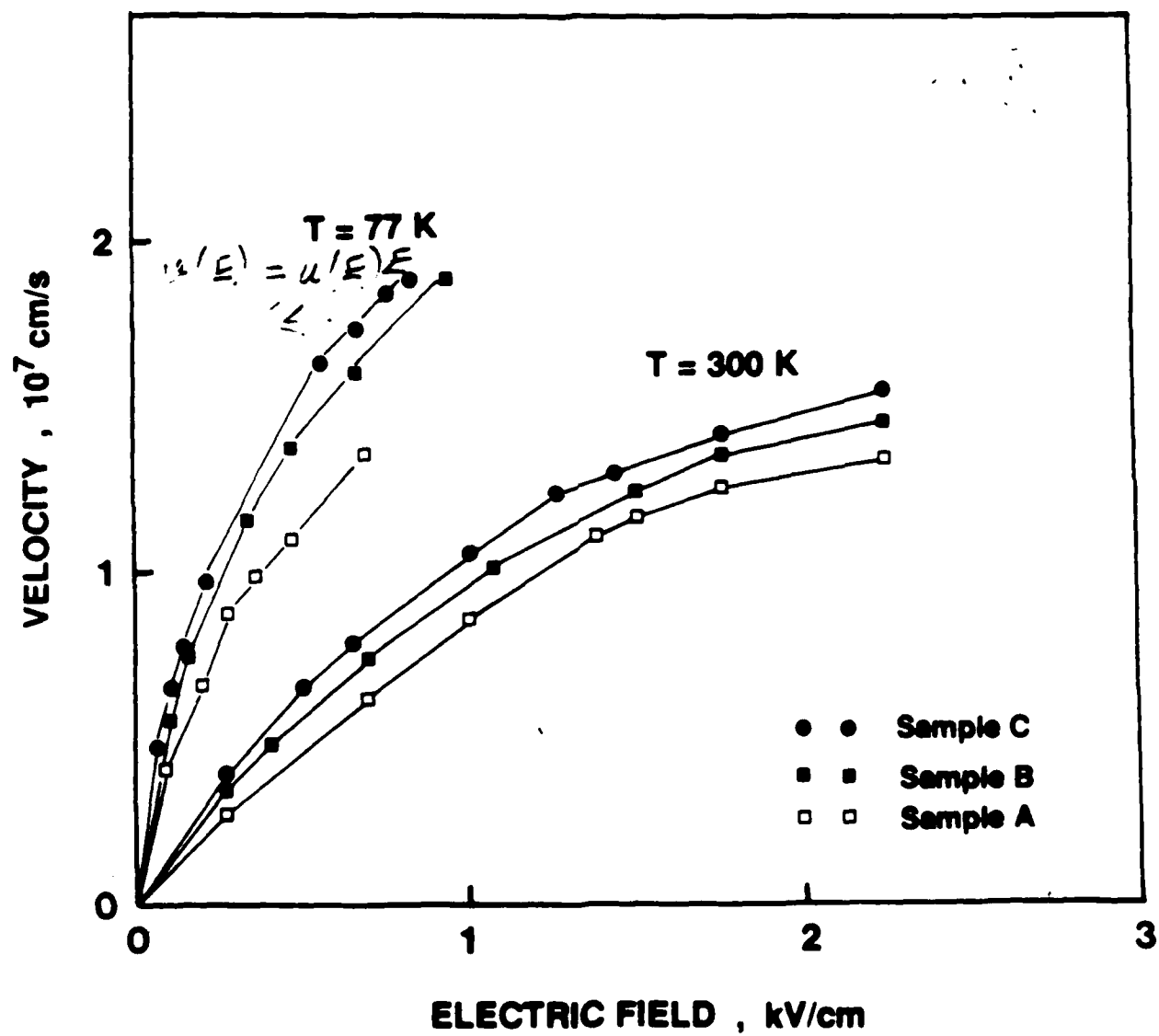
Table I. Measured Hall Data from $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ Heterostructure

Sample	Channel Composition	Mobility(cm²/Vs)		2DEG Density ($10^{12}cm^{-2}$)	
		300K	77K	300K	77K
A	0.53	11,500	50,100	1.65	1.60
B	0.60	12,300	65,200	1.79	1.74
C	0.65	13,900	74,000	1.82	1.79

Table II. Transport Data obtained from Hall and Shubnikov-de Haas (SDH) Measurements

Sample(x)	Hall Data at 4.2K		m^*/m_0	N_0[a]	N_1[b]	E_1-E_0[c]
	μ_H(cm²/Vs)	n_H($10^{12}cm^{-2}$)		($10^{12}cm^{-2}$)		(meV)
A(0.53)	67,900	1.46	0.046±0.002	1.12	0.26	43.2
B(0.60)	95,000	1.65	0.046±0.002	1.53	0.04[d]	76.1
C(0.65)	134,000	1.65	0.046±0.002	1.65	0.04[d]	84.6

a) Lowest subband occupation at 4.2K determined from SDH measurements.

b) Occupation in first excited subband at 4.2K

c) Energy separation between ground state and first excited state in the 2DEG.

d) These values are approximate.

In$_{0.65}$Ga$_{0.35}$As/In$_{0.52}$Al$_{0.48}$As MODFET

ID (mA)   GM (S)

MARKER(- .4000V , 11.34mA , 34.2E-03)

35.00   35.00 E-03

3.500 /div   3.500 /div

.0000   .0000
-1.800   0   .9000
      VG   .3000/div   (V)

$In = 65\%$ $150 \, \text{Å} \, QW$
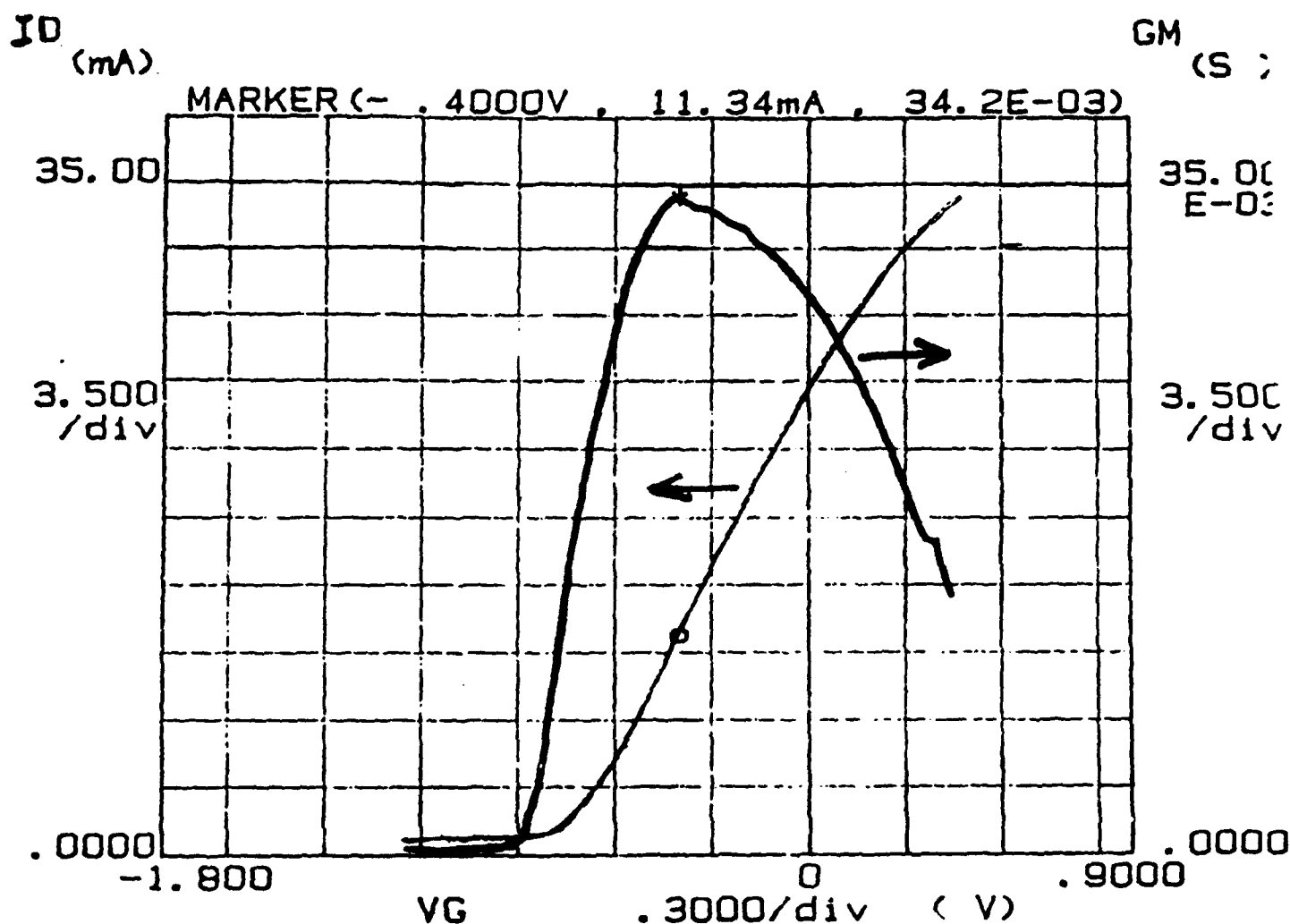
ϵ : $1.4 \mu m \times 75 \mu m$

Max current density : $450 \, mA/mm$
                        at $V_g = 0.4 V$.

G_m : 5 mS $V_c = 2 V$.

$\tau_m (ext) = 600 \, m$ $\gamma_{ds} = 5 mS$

345
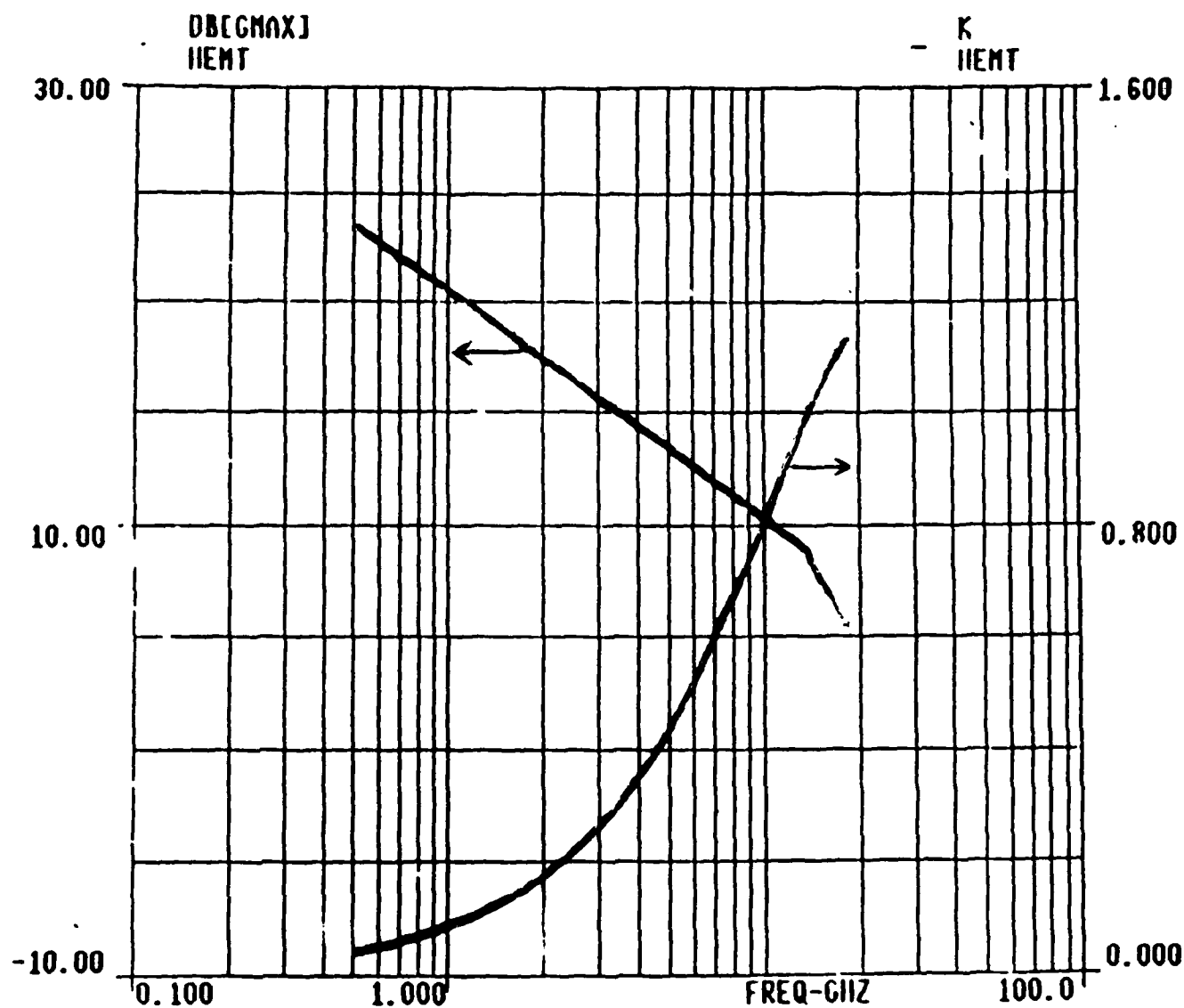
Max stable gain : 9 dB at 13.5 GHz
         MAG   : 5.5 dB at 18 GHz.

$f_T(int) = g_{mo}(HF)/2\pi C_{gs} = 38.6 \, GHz.$

346

$$n_{2DEG} = 1.7 E12 \ cm^{-2}$$

$$\mu_{300K} = 8500 \ cm^2/V.s.$$

$$\mu_{77K} = 22,000 \ cm^2/V.s.$$

IO (mA)   GM (S)

MARKER(- .5500V , 29.32mA , 27.6E-03)

60.00   30.00
                                           E-03

8.000   3.000
/div   /div

.0000   .0000
-1.400   0   .4000
      VG   .2000/div (V)

35.00

DB[H21]
UNV74003

15.00

-5.000
     1.000   10.00   FREQ-GHZ   :30 9

348
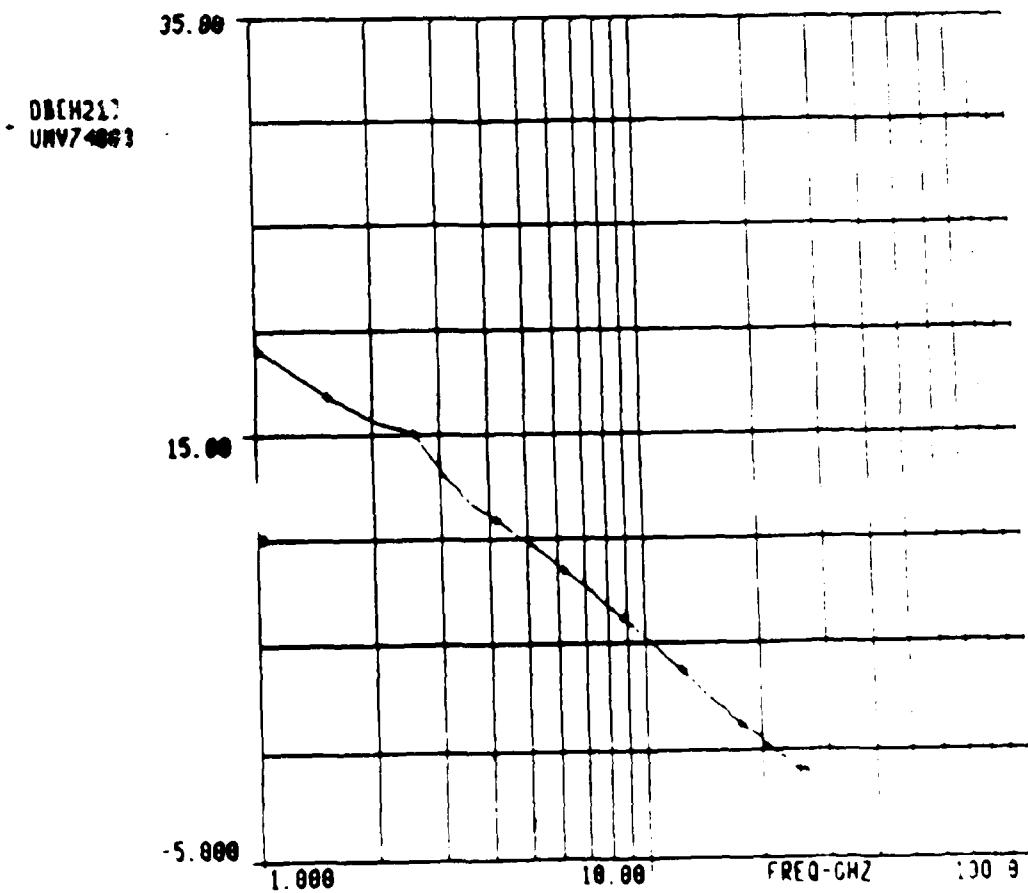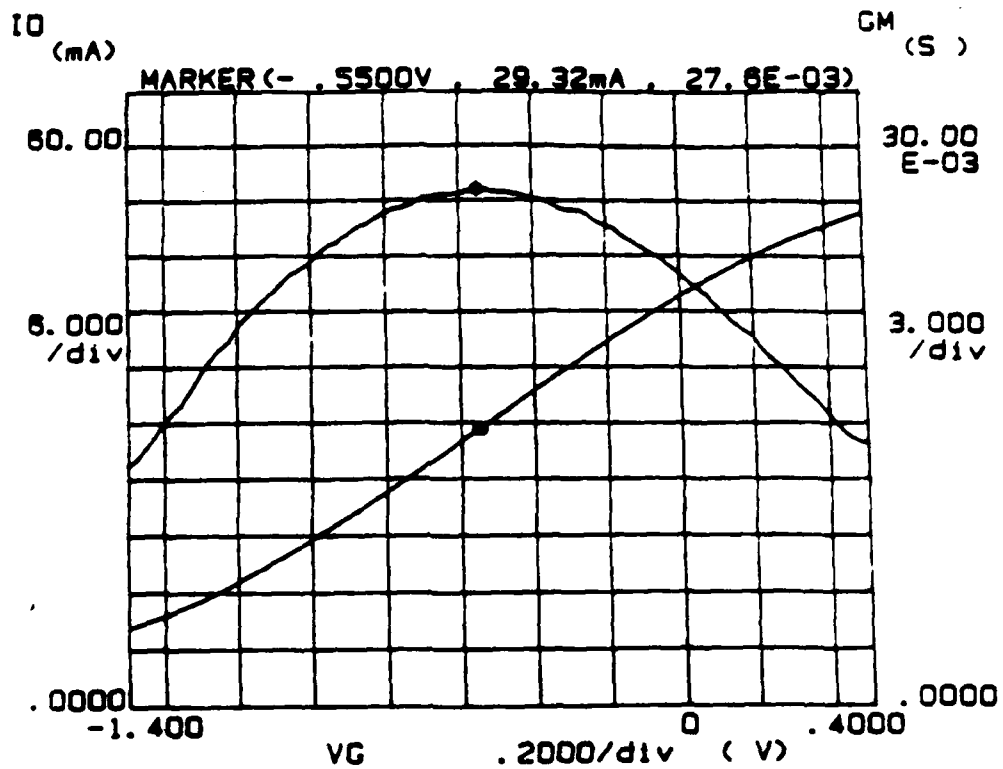
VI.   Quantum Wells Under Tensile Strain

STRAINED QUANTUM WELLS : TENSILE STRAIN
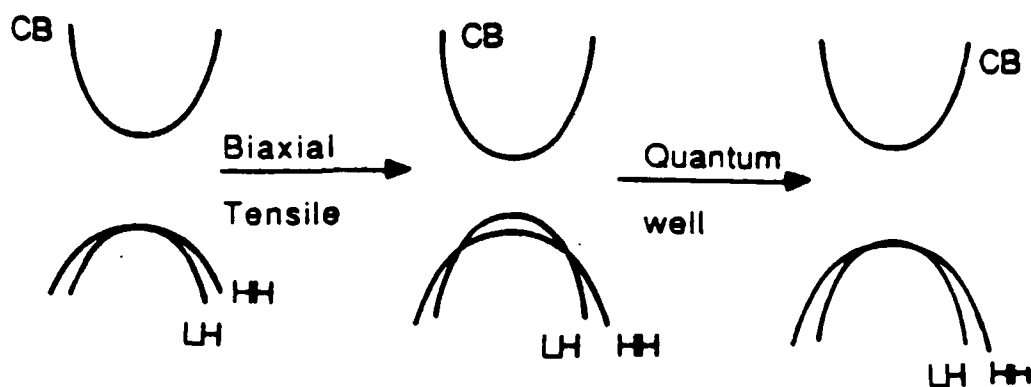
BULK	LH STATE ABOVE HH STATE	DEGENERACY RESTORED
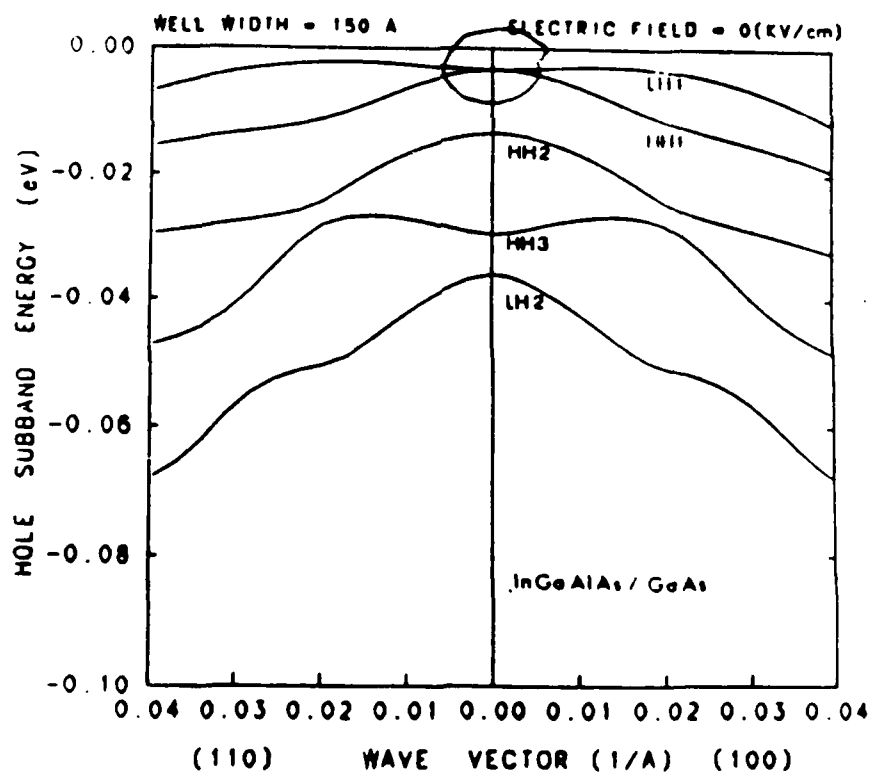
Hole dispersion relation for 150 Å

GaAs/In$_{0.06}$Ga$_{0.57}$Al$_{0.37}$As QW with degenerate

LH, HH states

ABSORPTION SPECTRA OF GaAs/$In_{0.06}Ga_{0.57}Al_{0.37}$As MQW
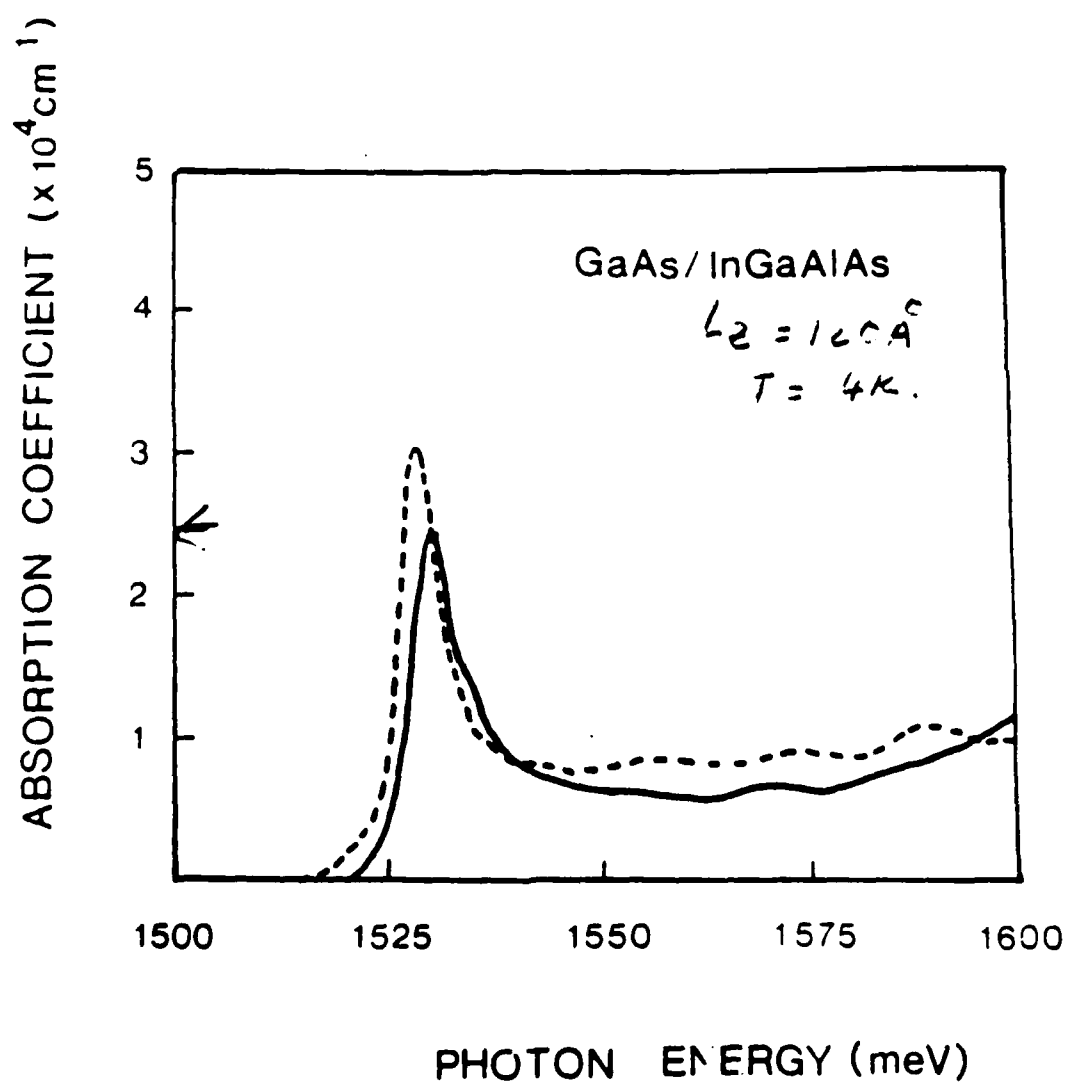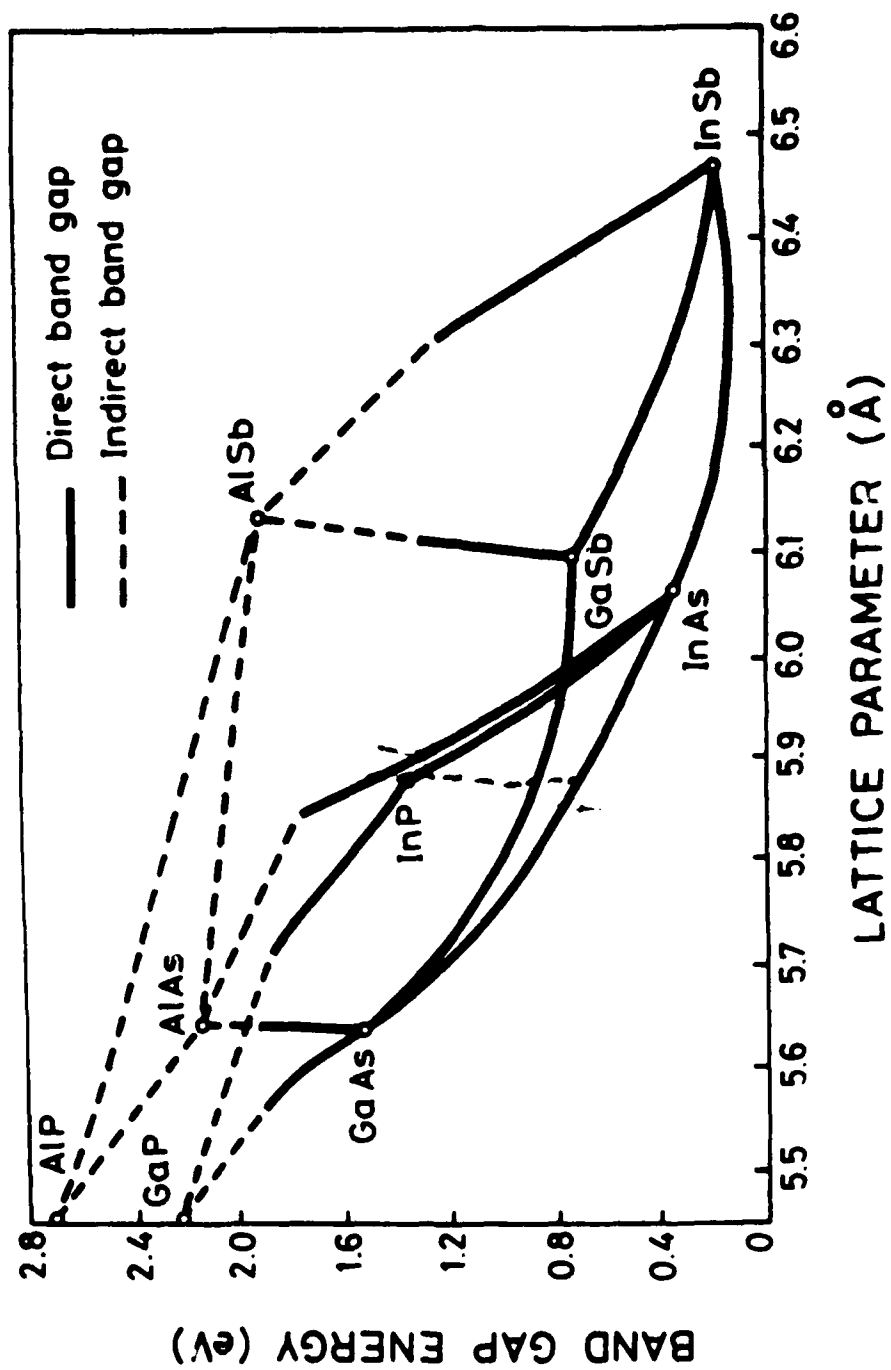
Quantum Wells With Biaxial Tensile Strain: Applications

1. Modulators   MQW
                 FETOM

2. Detectors

3. Sources – band-edge optical oscillator strengths can be enhanced by ~ factor of 2.

V. Growth and Properties of InP-based Resonant Tunneling Diodes

InGaAs / InAlAs / InP RT Diodes
45Å/61Å/45Å

Sample C

UMV 569

T = 300 K

$PTV = 6.1$

$J_p = 1 \times 10^4 \, A/cm^2$

$V_p = 385 \, mV$

185 meV

Current [mA]

Voltage [V]

UMV 569

T = 77 K

$PTV = 22$

Current [mA]

Voltage [V]
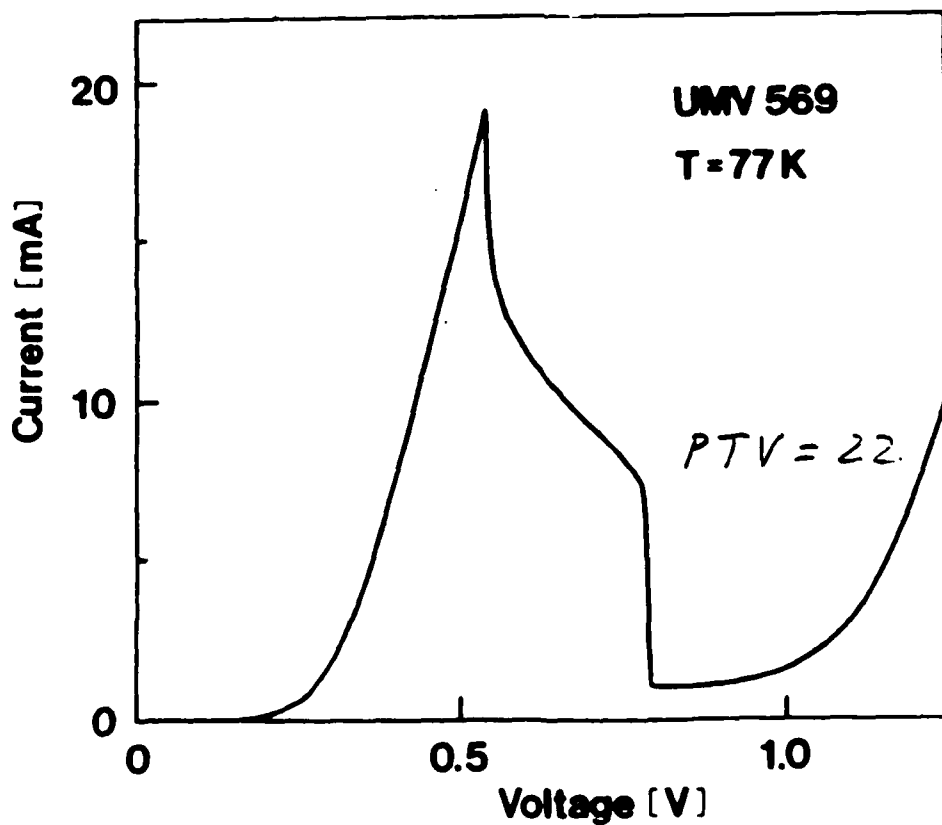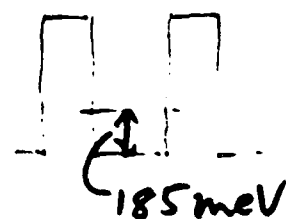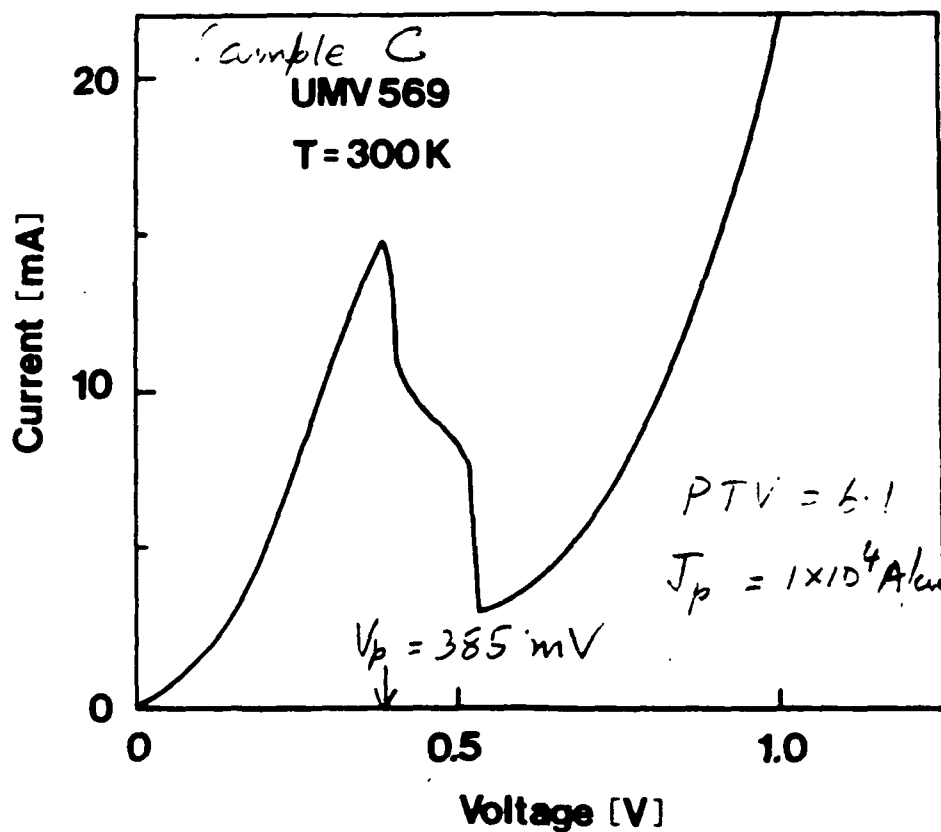
InGaAs / AlAs / InP RT Diode

200 Å	Si : $In_{0.53}Ga_{0.47}As$	5×10^{18}	
0.3 μm	Si : $In_{0.53}Ga_{0.47}As$	2×10^{18}	
50 Å	i – $In_{0.53}Ga_{0.47}As$		
23.7 Å	i – AlAs	barrier	B
44.0 Å	i – $In_{0.53}Ga_{0.47}As$	well	W
23.7 Å	i – AlAs	barrier	B
50 Å	i – $In_{0.53}Ga_{0.47}As$		
0.3 μm	Si : $In_{0.53}Ga_{0.47}As$	2×10^{18}	
10 period InGaAs/InAlAs superlattice			
S-doped n^+ InP Substrate			
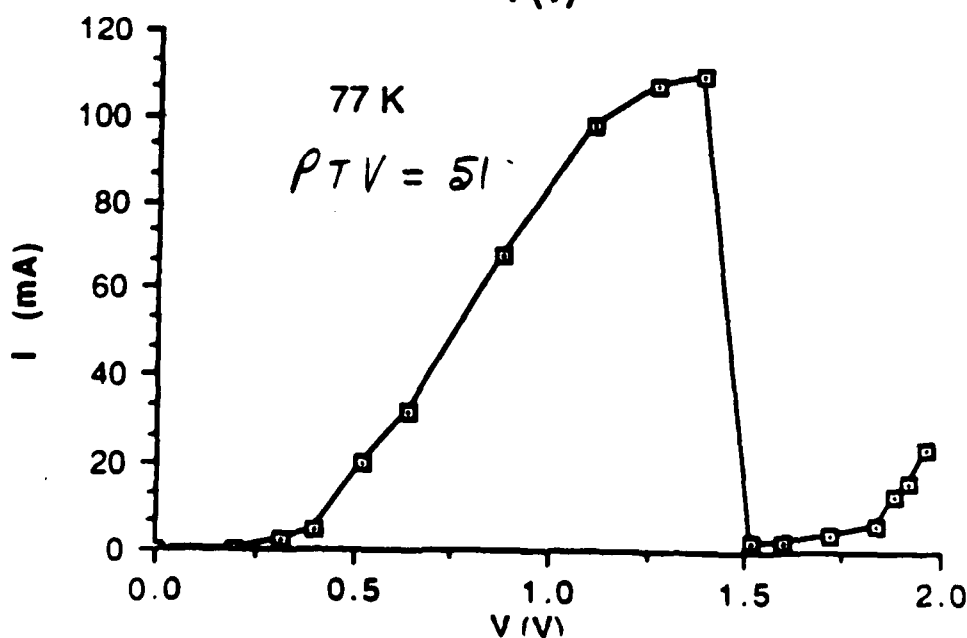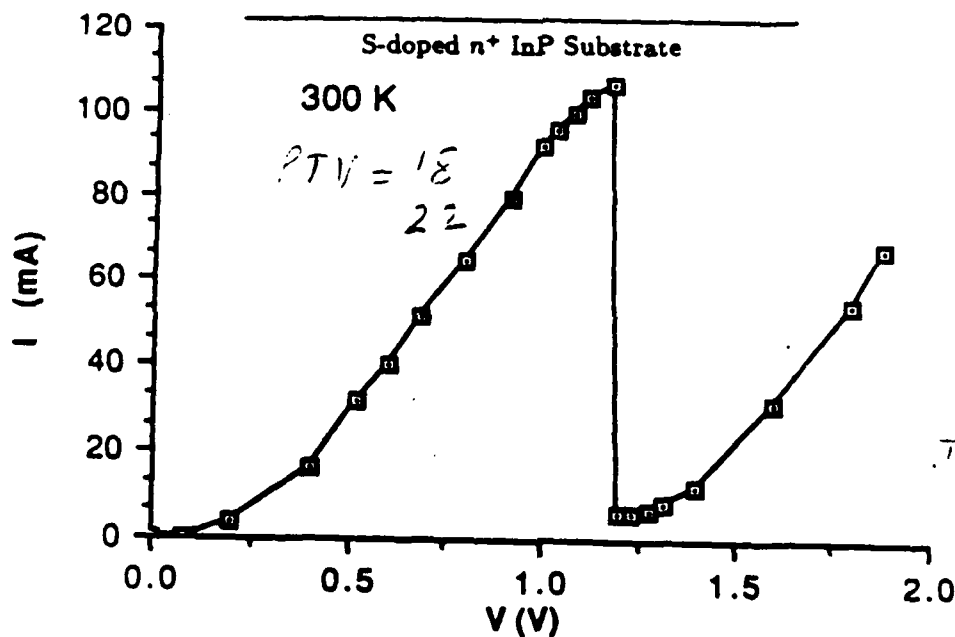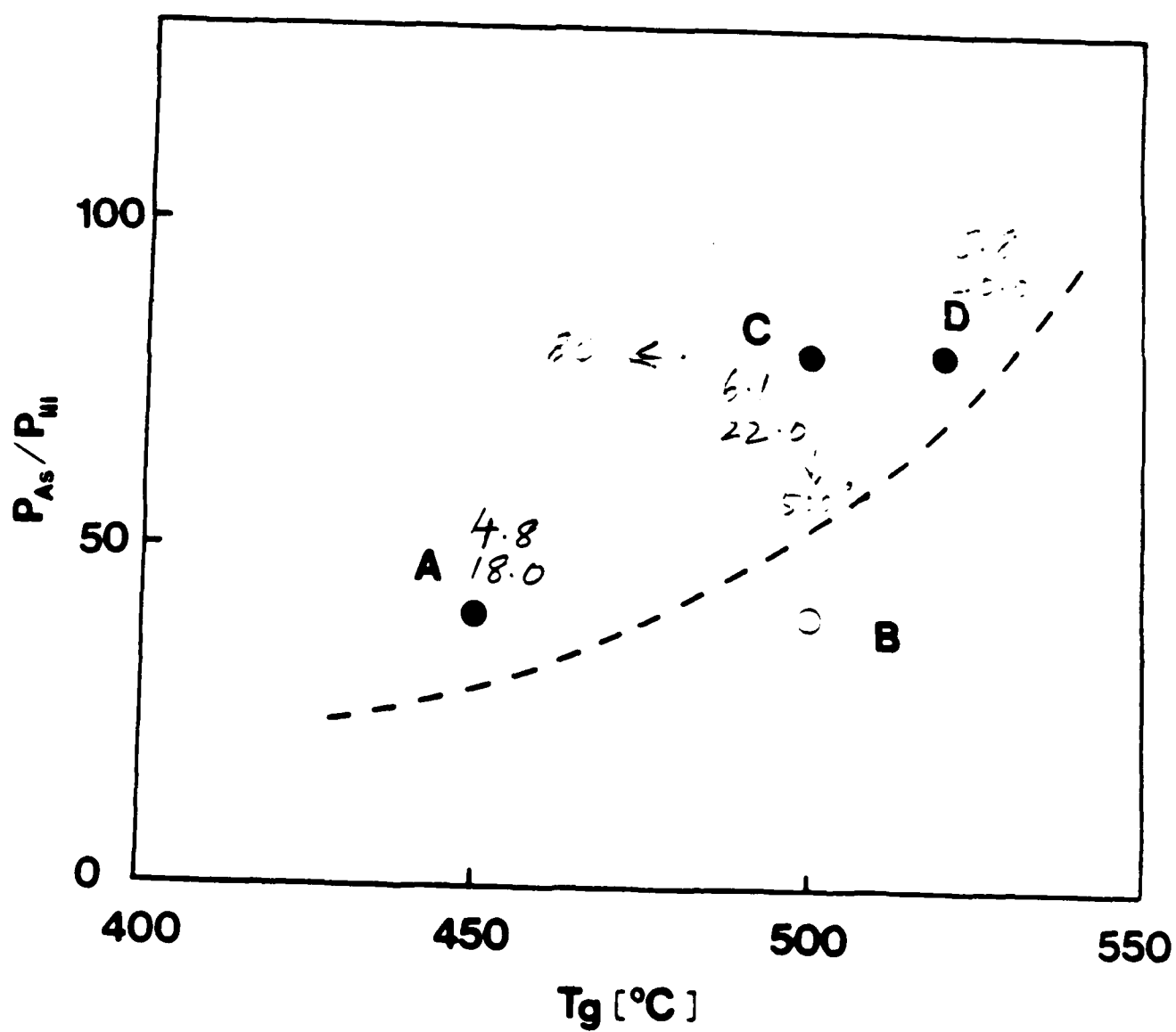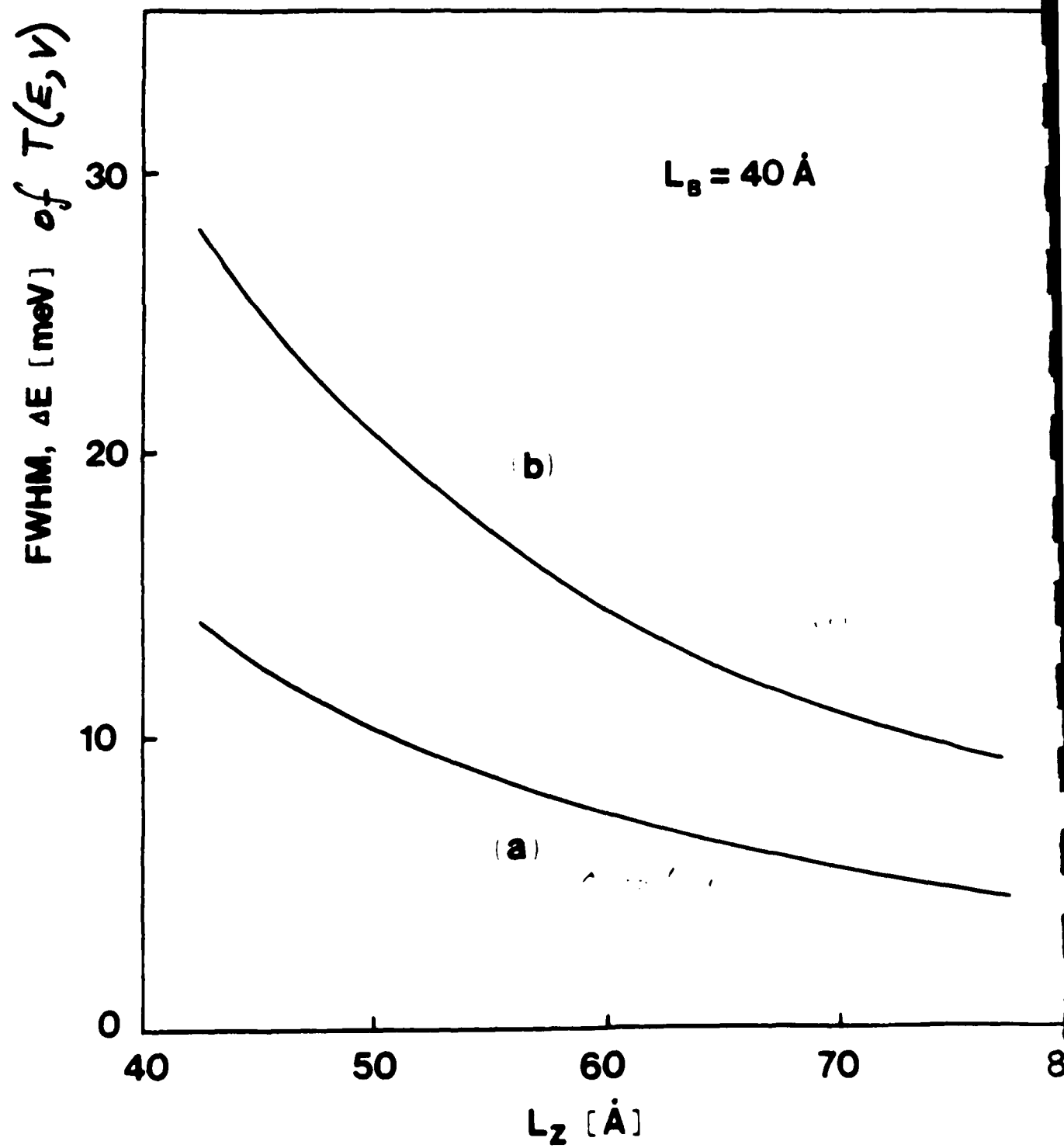
300 K

$PTV = 18$
2.2

$J_c = 1.5 \times 10^4 A/cm^2$

77 K

$PTV = 51$

356

A DIFFUSED JUNCTION InP JFET FOR HIGH SPEED INTEGRATED CIRCUIT AND POWER APPLICATIONS

C. R. Zeisse, R. Nguyen, T. T. Vu, L. Messick, and K. L. Moazed*

Electronic Material Sciences Division (Code 56)
Naval Ocean Systems Center
San Diego, CA 92152-5000

*Department of Material Science
North Carolina State University
Raleigh, NC 27695-7916

A Diffused Junction InP JFET for High Speed Integrated Circuit and Power Applications

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San Diego, CA 92152-5000   Raleigh, NC 27695-7916

Junction field effect transistors have been made by selective diffusion of zinc into InP channel layers. Devices with an epitaxial channel have a transconductance of 120 mS mm-1, the highest reported to date.

Zinc diffusion for the gate was carried out in a closed ampoule using a source of powdered Zn2As3. The temperature was 535C for 4 minutes followed by a quench in water. This produced a hole concentration of (1-2) E18 cm-3 to a depth of 0.5 microns in a Si implanted layer of electron concentration (mid-high) E16 cm-3 and total thickness 0.8 microns. The diffusion was masked by SiO2. The gate opening was 1.5 microns by 250 microns. Source-drain metallization was AuGe (0.2 microns). Gate metallization was unalloyed Ti/Au (0.1 microns/.25 microns). The dc characteristics of this device show a transconductance of 20 mS (80 mS mm-1) at Vgs = 0 V and a gate to source leakage of 100 nA at Vgs = -2 V.

Zinc was also diffused into an InP channel (1E17 cm-3, 0.45 microns) epitaxially grown on a 0.5 micron undoped buffer layer. Diffusion was quenched after 2 1/4 minutes at 540C, producing a 0.2 micron thick gate layer with a hole concentration of (1-2) E18 cm-3. This time the gate opening was 1.6 microns by 200 microns. Devices were isolated with a mesa etch. The characteristics are shown below. The transconductance is 24 mS (120 mS mm-1) for Vgs between 0 V and 0.7 V. The output resistance is 9 kohm at Vgs = -1 V. The saturated drain to source current was 150 +- 10 mA from one device to the next over a wafer 10 mm on a side. The dc drift is 3% or less in 1E5 s.

The best dc characteristics and the lowest leakage have not yet been brought together in the same device, although there is no fundamental reason why this can not be done. The InP JFET is a stable device with high gain, low output conductance, low leakage, and good wafer uniformity, features required for many electro-optic and power applications.

L = 2 μm

W = 200 μm
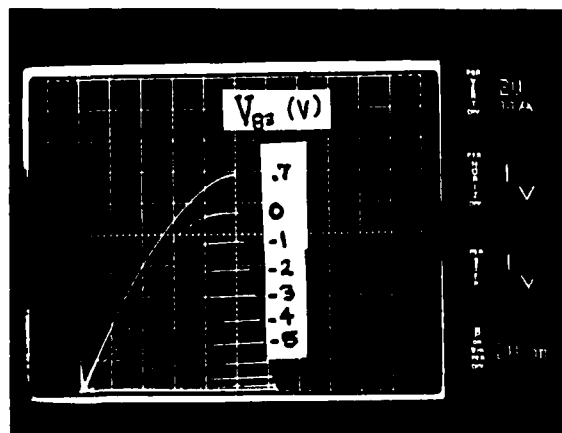
NOSC

Integrated InGaAs Photodetector —
InP Transimpedance Amplifier Circuit

Semi-Insulating Substrate

0.5 μm

0.5 μm

1.6 μm

0.8 μm

n+

p+

n

n+

InP JFET
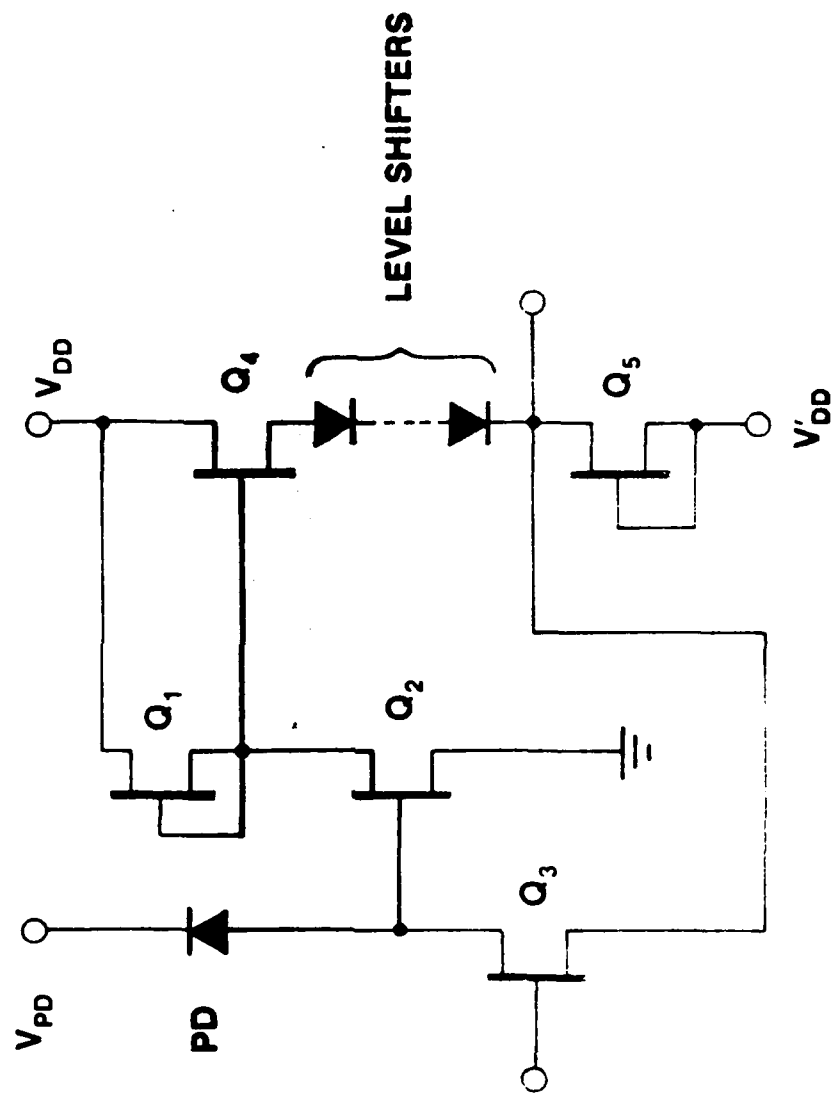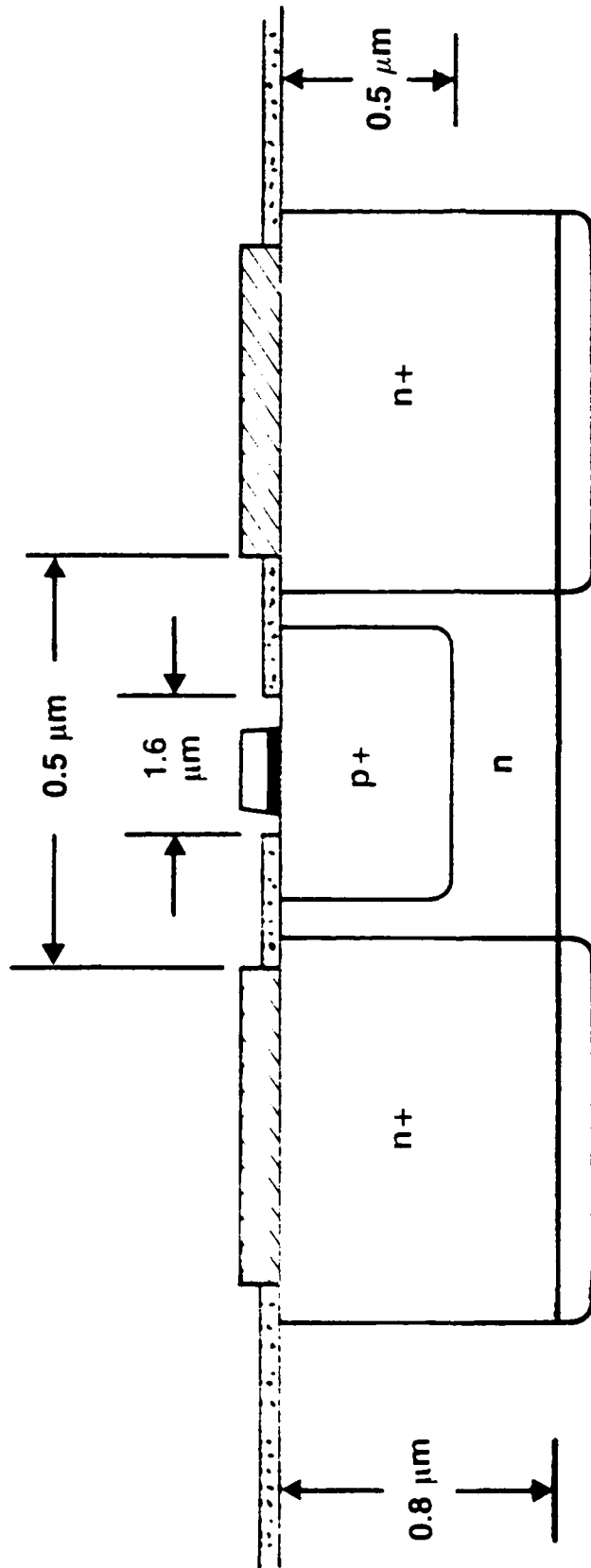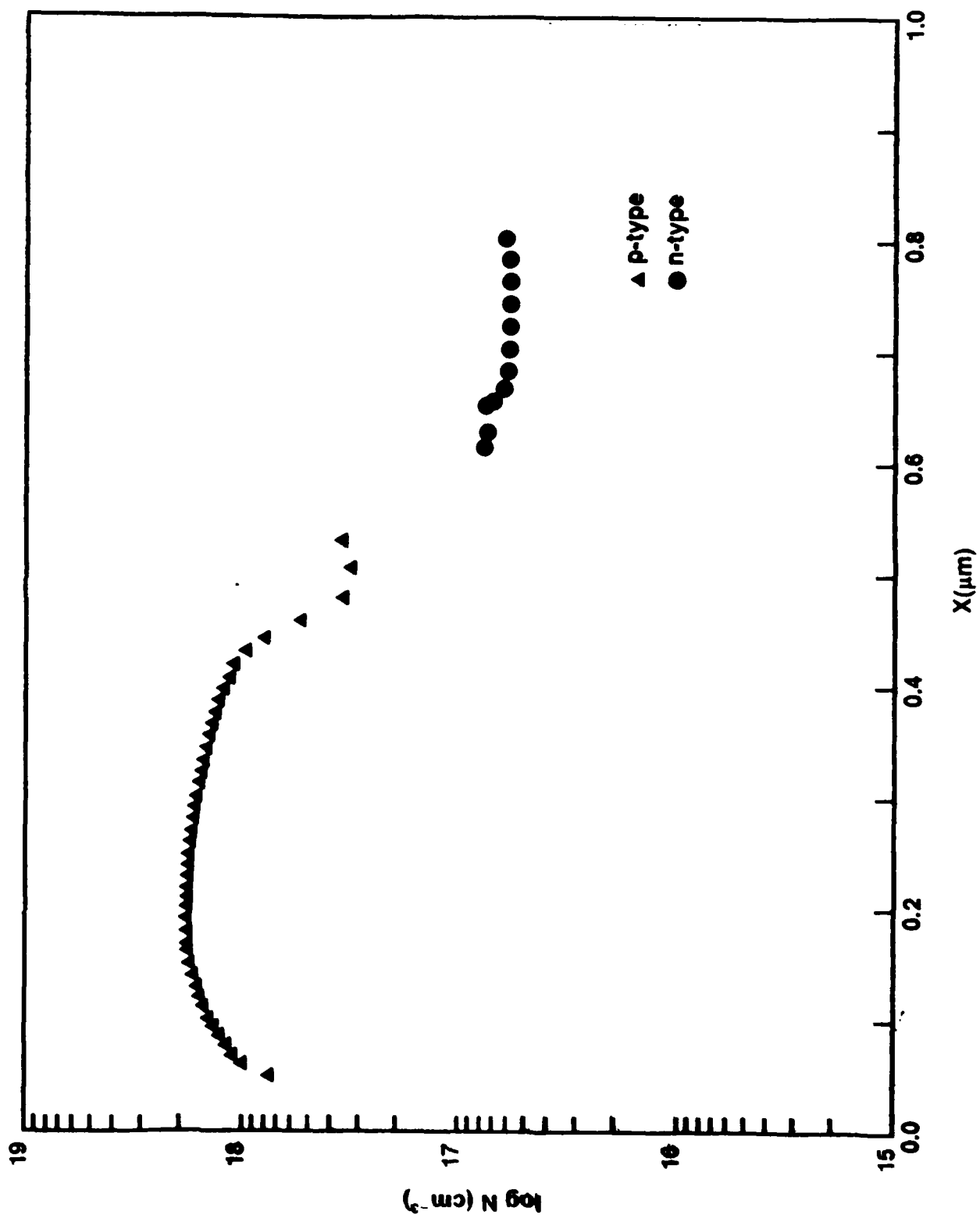
SOURCE
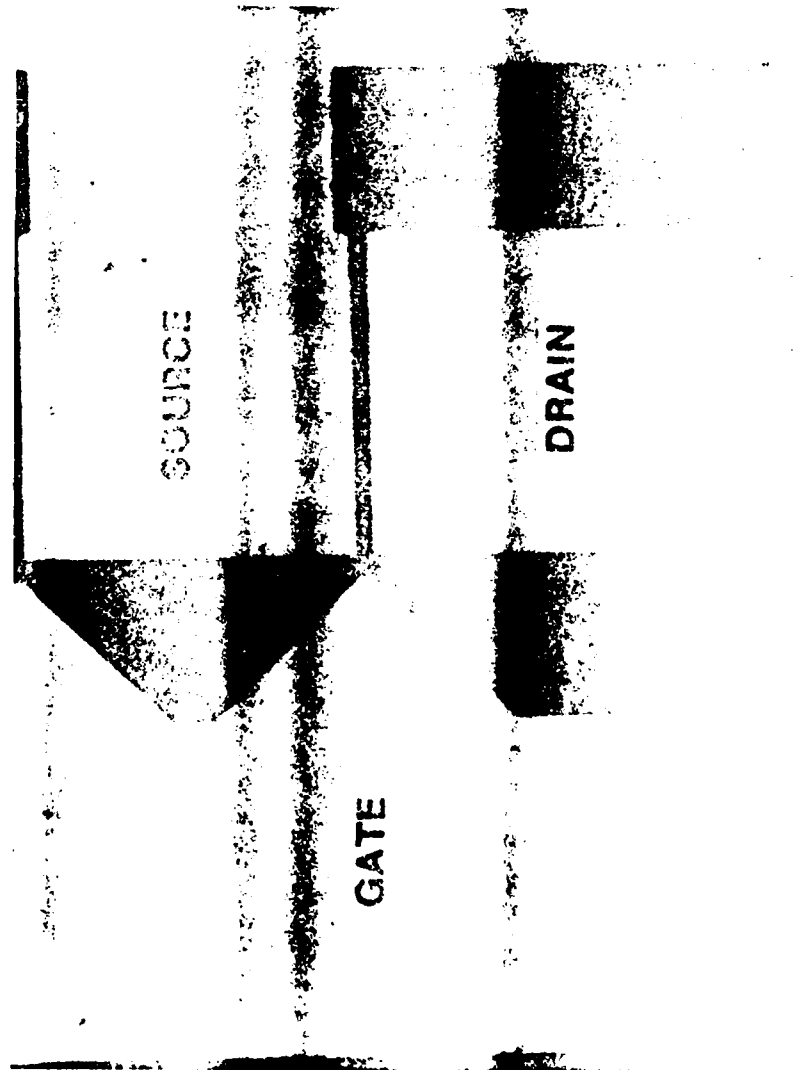
GATE

DRAIN

PLAN VIEW

NOSC

InP JFET
Implanted Channel

L = 2.5 μm
W = 250 μm
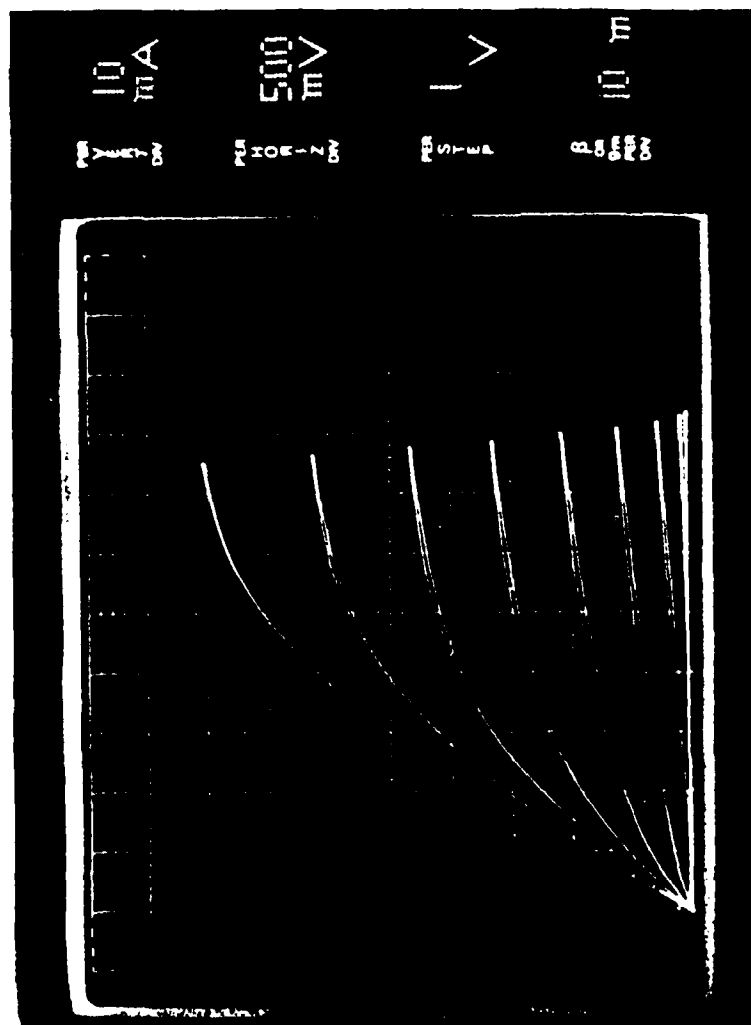
$g_m/W = 80$ mS mm^{-1}

NOSC

InP JFET
Implanted Channel

GATE TO
SOURCE
LEAKAGE

L = 2.5 μm
W = 250 μm

Ti/Au (0.1 μm/0.25 μm)

AuGe (0.2 μm)

SiO₂ (0.1 μm)

n Channel

Undoped Buffer

Simi-Insulating Substrate

p⁺

8 μm

1.6 μm

0.45 μm

0.50 μm

NOSC

368

SOURCE

DRAIN

GATE

NOSC R2
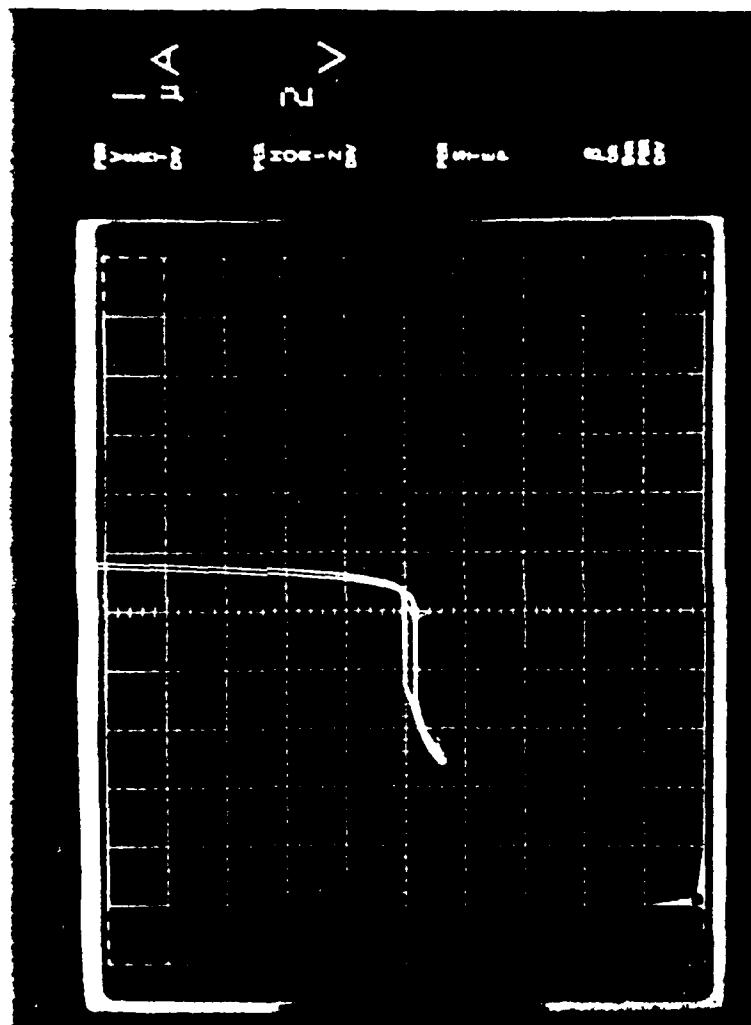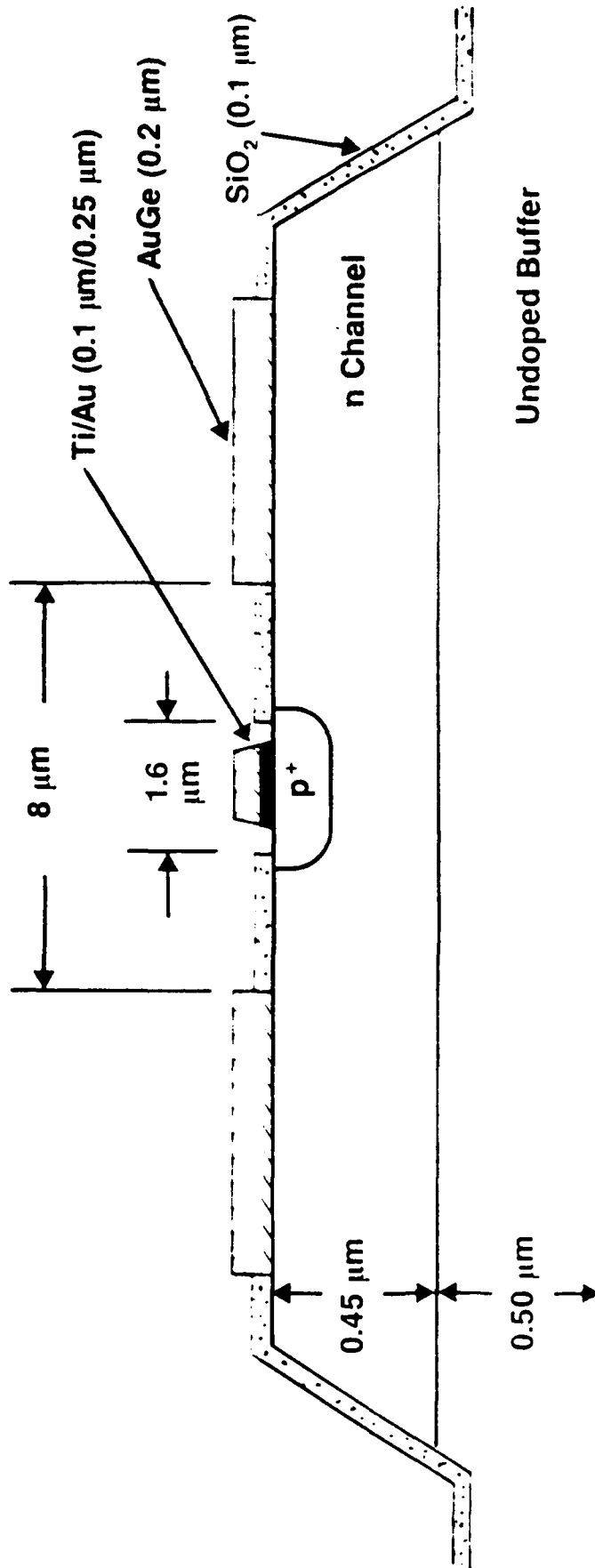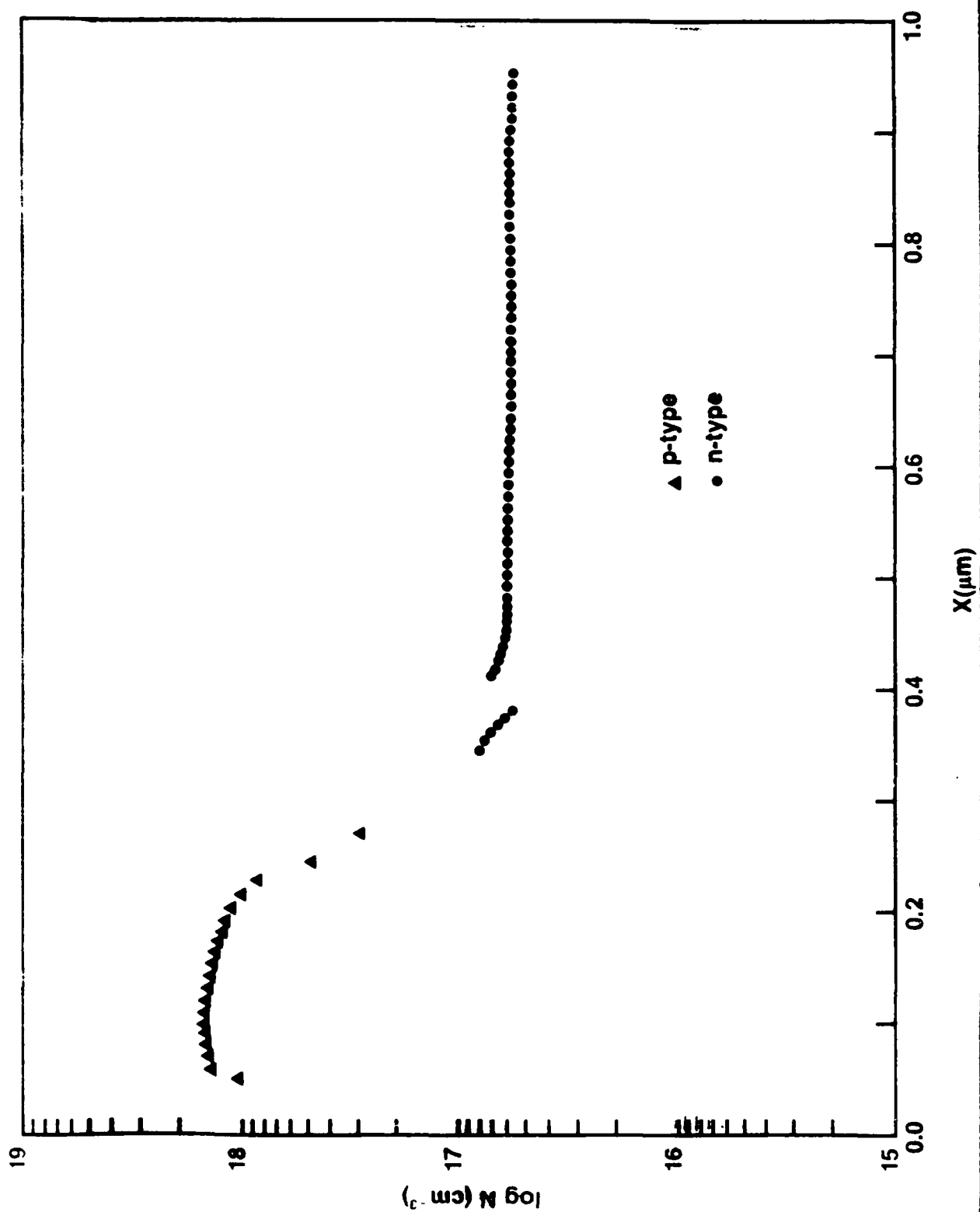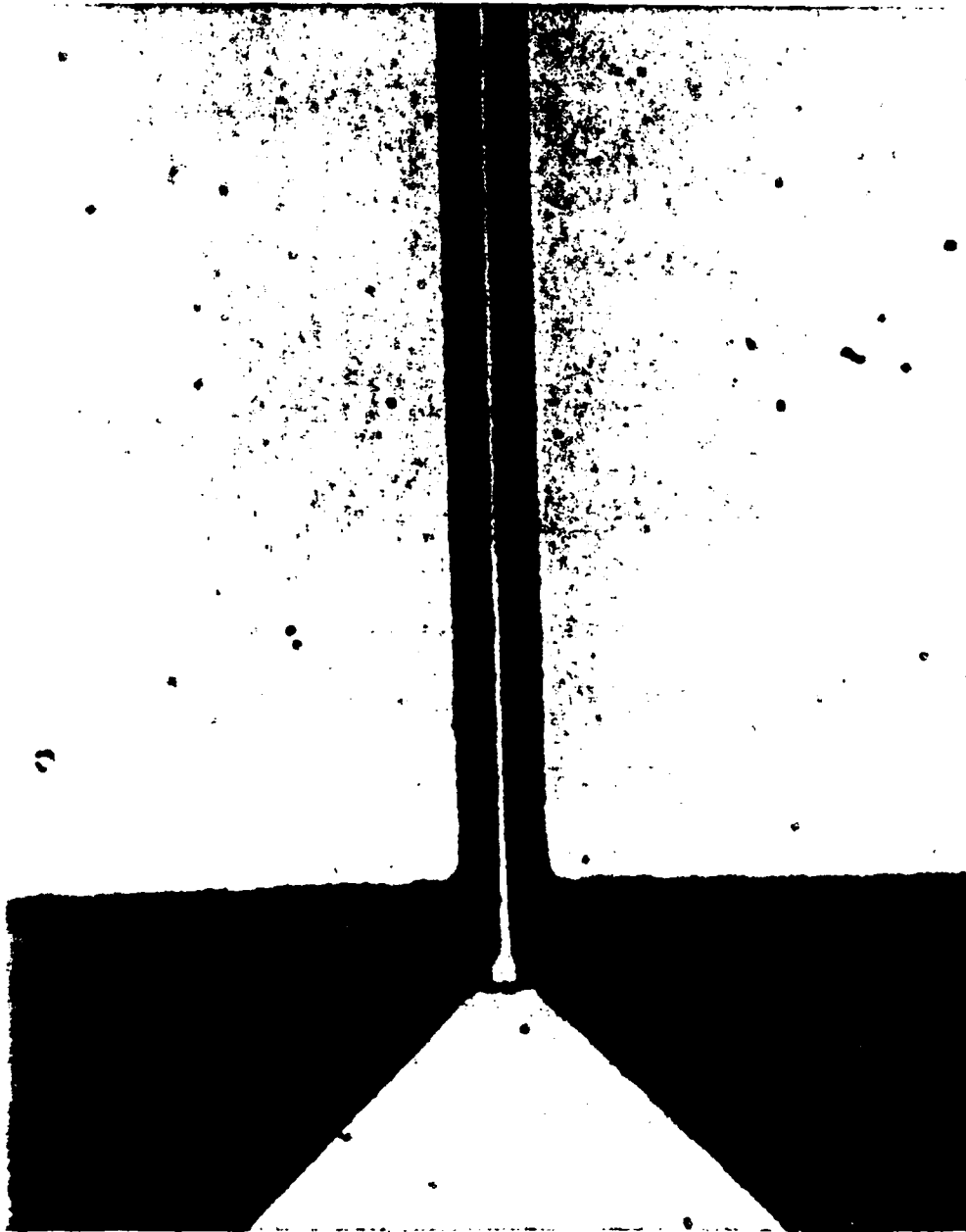
InP JFET
Epitaxial Channel
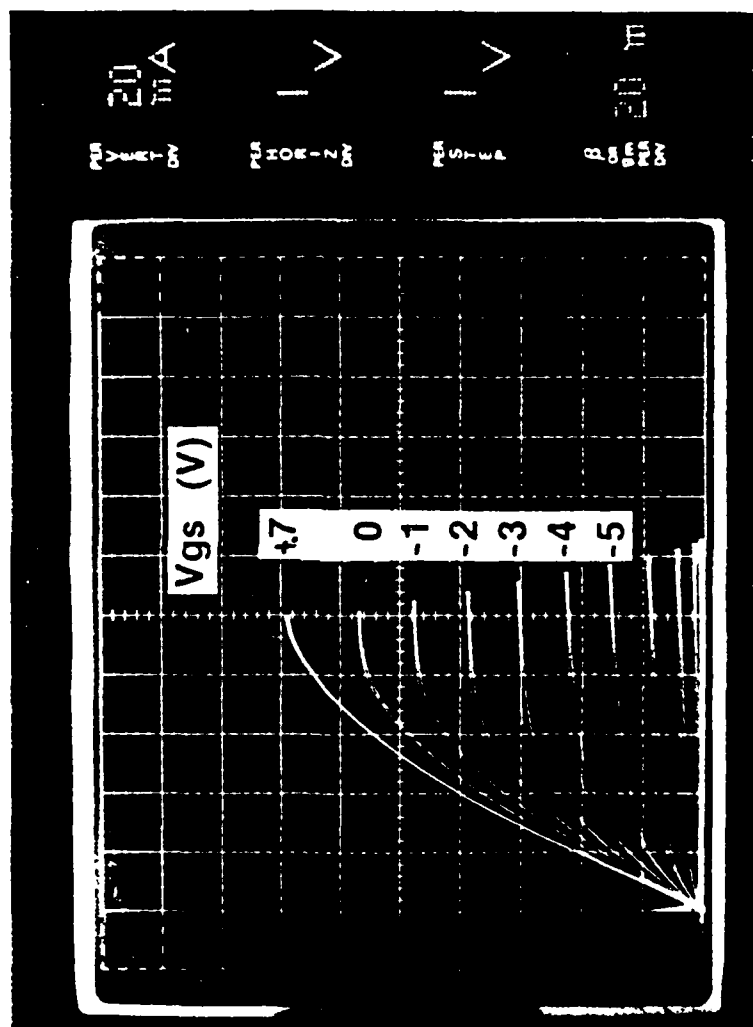
Vgs (V)

+.7
0
-1
-2
-3
-4
-5

L = 2μm
W = 200 μm

$g_m/W = 120$ mS mm^{-1}

NOSC

EPITAXIAL Channel
L = 2μm
W = 200 μm

V_{ds} = +4.00 V
V_{gs} = –1.000 V

JFET Drift

2.8†

t(S)

I_{ds} (mA)

372

InP JFET

EXTRINSIC TRANSCONDUCTANCE (m^{-1} mm^{-1})

CHANNEL DOPING (cm^{-3})
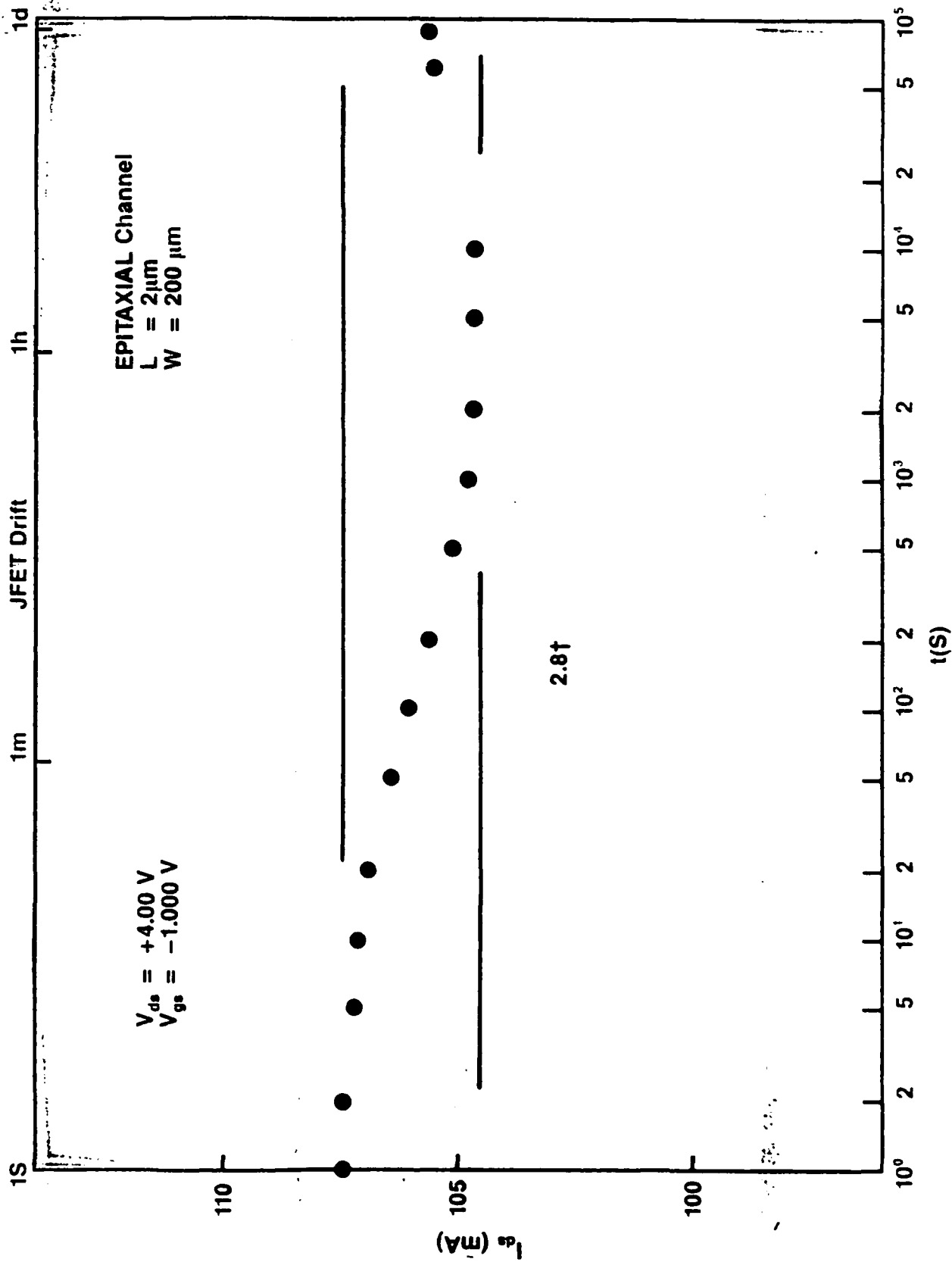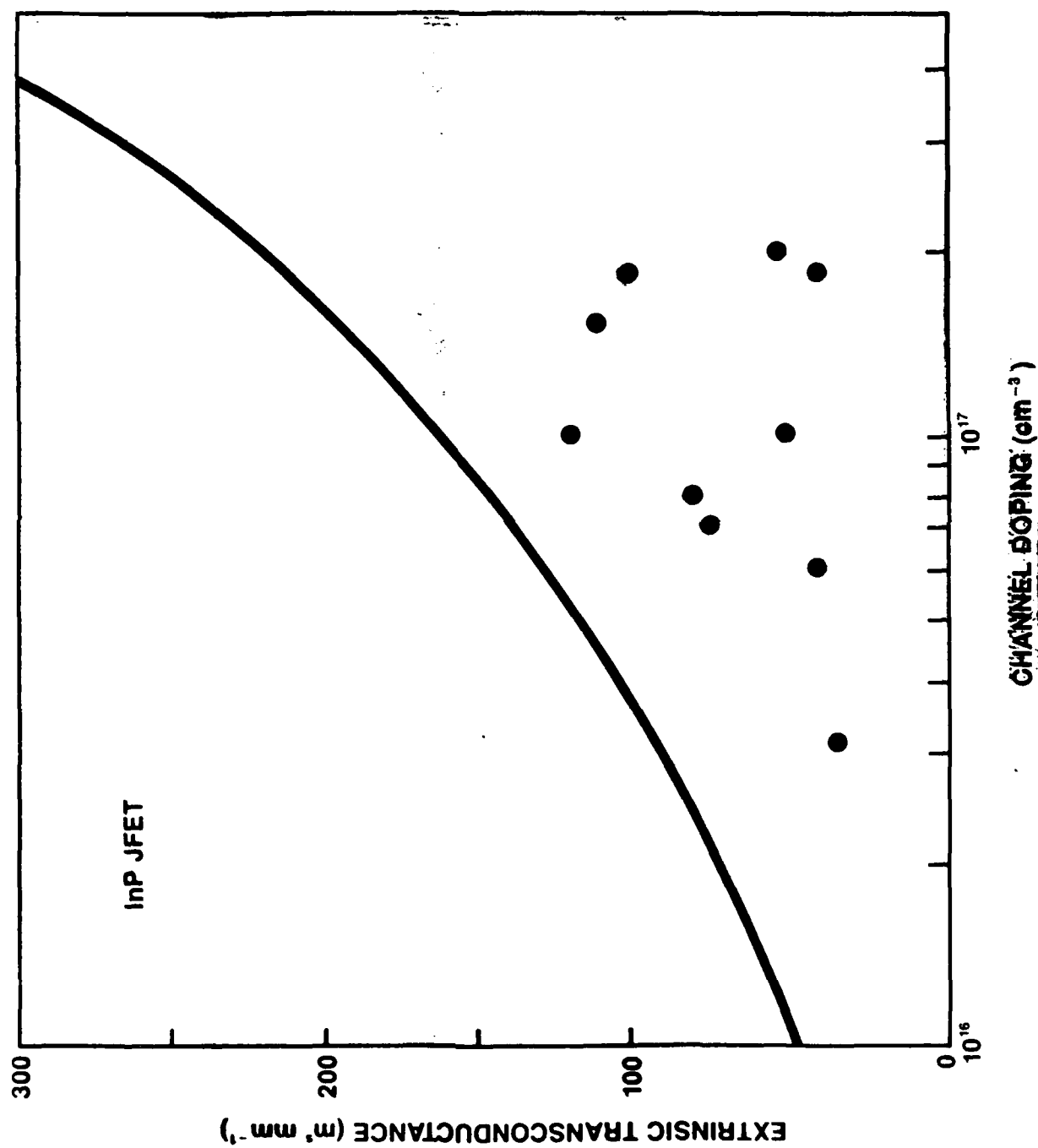
RADIATION EFFECTS ON InP BASED ELECTRICAL AND OPTICAL DEVICES

K. N. Vu, J. Y Yaung and R. E. Helander

TRW/DSG
Systems Engineering and Development Division
Carson, CA

Radiation Effects on
InP Based
Electrical and Optical Devices

K. N. Vu
J. Y. Yaung
R. E. Helander

TRW/DSG

System Engineering and Development Division

Outline

* Introduction
* HEMT Device
* HBT Device
* Solar Cells
* Conclusion
* Recommendations

Introduction to Radiation Effects in Materials

- **Dose Rate Effects**

  - Conductivity Modulation ($\downarrow R_{bulk}$ or $\uparrow I_{shunt}$)

  - Photocurrent across semiconductor junctions ($\uparrow I_{photo}$)

  - Radiation-Induced Backgating (ΔV_{th} and long-term transient)

- **Total Dose Effects**

  - Charge trappings in the dielectric and interfaces (ΔV_{th} and $\uparrow I_{leakage}$)

  - Minority carrier lifetime reduction ($\downarrow \beta$)

  - Carrier Removal (ΔV_{th}, $\uparrow R_s$, and $\uparrow R_b$)

  - Mobility degradation ($\downarrow g_m$)

- **Neutron Effects**

  - Minority carrier lifetime reduction ($\downarrow \beta$)

  - Carrier removal (ΔV_{th}, $\uparrow R_s$, and $\uparrow R_b$)

  - Mobility degradation ($\downarrow g_m$)

HEMT Device

Radiation Effects in AlGaAs and InGaAs HEMT

AlGaAs HEMT

SOURCE GATE DRAIN GaInAs HEMT

CAP BARRIER CAP

CHANNEL

BUFFER

SUBSTRATE

AlGaAs HEMT	GaInAs HEMT
N+ GaAs	N+ $Ga_{.47}In_{.53}As$
N+ $Al_{.3}Ga_{.7}As$	N $Al_{.48}In_{.52}As$
P- GaAs	N- $Ga_{.47}In_{.53}As$
P- GaAs	N- $Al_{.48}In_{.52}As$
SI GaAs	SI InP
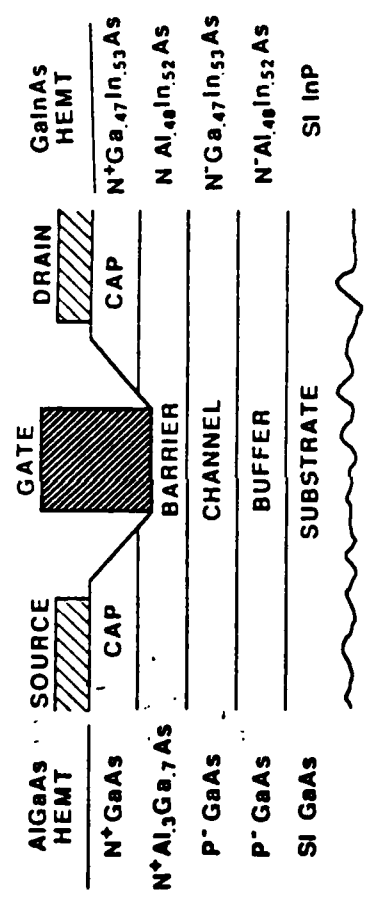
Radiation Environment	HEMT	
	AlGaAs	InGaAs
Dose Rate (rad(material)/sec)	$\sim 10^{10}$ (digital) $\sim 10^{11}$ (linear)	$< 10^{10}$ (digital) $> 10^{11}$ (linear)
Total dose (rad (material))	$\sim 10^{8}$	$\sim 10^{9}$
Neutron (n/cm^{2})	$\sim 10^{15}$	$\sim 10^{15}$

[1] IEEE Transactions on Nuclear Science, December 1985 and 1987

[2] 1rad (GaAs) ≈ 1rad (InP)

Primary Concern in HEMT

- **Dose Rate Effects**

  - Define dose-rate upset or failure as

    $$I_{shunt} + I_{photo} >> I_{operating}$$

    - I_{shunt}-current flow b/t source-to-drain due to increase in bulk conductivity
    - I_{photo}-current flow due to drift and diffusion of electron-hole pair (EHP) across high potential junction.
    - $I_{operating}$-bias current

  - InGaAs HEMP digital applications-<u>lower</u> dose rate threshold due to higher generation EHP in InP

  - InGaAs HEMT high-power high frequency (linear) applications-<u>higher</u> dose rate threshold

    $$I_{operating} (InP) >> I_{operating} (GaAs)$$

  - Effects of radiation-induced backgating and long-term transient can be minimized using
    - buffer layer (superlattice)
    - improved processing methods

Secondary Concern in HEMT

- **Total Dose Effects**

  - Carrier removal and mobility degradation are the dominant total dose effects in HEMT
    - Carrier removal-change in threshold voltage
    - Mobility degradation-lower transconductance
    - Effects more significant in GaAs than InP

  - Minority carrier lifetime reduction-minimal in majority carrier device (HEMT)
  - Charge trappings effects is minimal in HEMT-no gate insulator

- **Neutron Effects**

  - Carrier removal and mobility degradation-dominant neutron effects
  - Minimal minority carrier lifetime reduction effects-majority carrier device
  - No data exist to assess neutron damaging effects in InP

HBT DEVICES

Radiation Effects in AlGaAs and InGaAs HBT

EMITTER

AlGaAs HBT
GaAs
AlGaAs
GaAs
GaAs
GaAs
GaAs

InGaAs HBT
(Ga,Al)InAs
AlInAs
$In_{.53}Ga_{.47}As$
$In_{.53}Ga_{.47}As$
$In_{.53}Ga_{.47}As$
InP

n+ n   p BASE   p   n-   n+ COLLECTOR

SI SUBSTRATE
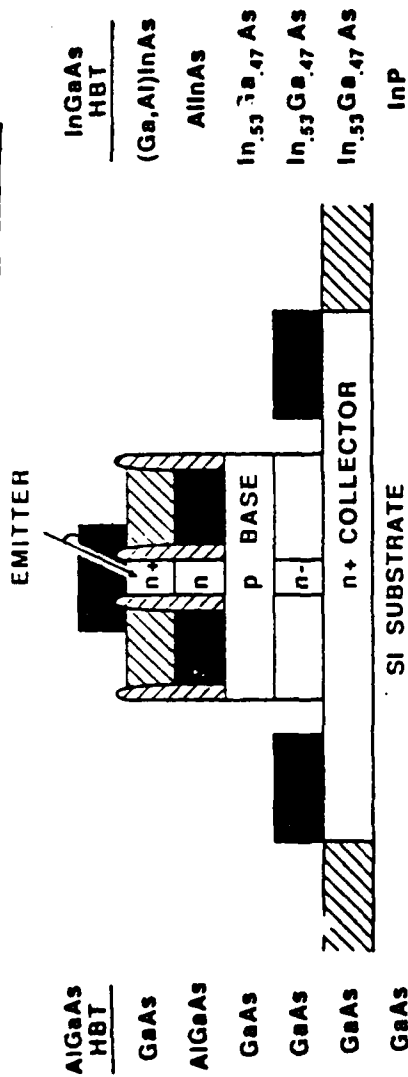
Radiation Environment	HBT	
	AlGaAs	InGaAs
Dose Rate (rad(material)/sec)	$\sim 10^{10}$ (digital)	$<10^{10}$ (digital) (estimated)
Total dose (rad (material))	$\sim 10^{8}$	$\sim 10^{9}$ (estimated)
Neutron (n/cm^2)	10^{14}-10^{15}	10^{14}-10^{15} (estimated)

Primary Concern in HBT

- **Neutron Effects**

  - Minority carrier lifetime reduction is the dominant neutron effect

    - increase in recombination current
    - increase in base current ideality factor
    - decrease in current gain

  - Carrier removal and mobility degradation are secondary neutron effects

    - increase in base resistance (R_b)
    - decrease in maximum frequency of oscillation (f_{max})
    - decrease in extrinsic transconductance (g_m)

  - No data exists to assess neutron damage effects in InP HBT

Secondary Concern in HBT

- **Dose Rate Effects**

  - Photocurrent maybe the dominant dose rate effect in HBT due to Beta-multiplied photocurrent.

  - Conductivity Modulation effects should be minimum due to
    - highly-doped n+ collector
    - approximately equipotential collector contacts b/t devices.

  - No long term transients were observed in TRW AlGaAs HBT test structure

  - InGaAs HBT digital applications-lower dose rate threshold due to higher generation EHP in InP than GaAs

  - InGaAs HBT linear applications-higher dose rate threshold due to higher InGaAs HBT biasing current

- **Total Dose Effects**

  - Damage Effects similar to neutron effects

  - Total dose damage effects are more significant in GaAs than InP

  - No charge trappings were observed in TRW AlGaAs HBT test structure.

387

Conclusion

- InGaAs HEMT and HBT are ideal for high radiation requirements applications based on our study of InP material properties.

Recommendations

- Several tests should be undertaken to assess

  - neutron displacement effects in InGaAs devices
  - dose rate effects in InGaAs devices
  - SEU in InGaAs devices

- Additional radiation effects modeling are recommended to gain insights into further improving the radiation tolerances of InGaAs devices

  - processing simulator (SUPREME IV)
  - device simulator (SEDAN III, PISCES, BAMBI, and Monte Carlo simulator)
  - circuit simulator (SPICE)

InP Solar Cells

InP Solar Cell Configurations
(InP Cell)

n/p

AR COAT SiO
Au

n (S: >10^18/cm³)

p (Zn:4.6x10^16/cm³)

SUBSTRATE

0.068 µ
0.040 µ

BACK CONTACT: Au/Zn

GROWTH METHOD: OPEN TUBE CAPPED DIFFUSION

p/n

AR COAT Sb₂O₃
Au/Zn

GaInAs (Zn: 10^18/cm³)   0.065 µ

p (Zn:10^18/cm³)   0.5 µ

n (S: 10^16/cm³)   30 µ

n (S: 7x10^18/cm³)

SUBSTRATE

BACK CONTACT: Au/Sn

GROWTH METHOD: MOCVD

(Comparing GaAs Cell)

	n·p CELL	DOPANT	
TYPE	THICKNESS µm	ATOM	CONCENTRATION cm³
n	0.7	Se	1.5x10^18
p	3	Zn	7x10^17
p	.5	Zn	8x10^18

	p·n CELL	DOPANT	
TYPE	THICKNESS µm	ATOM	CONCENTRATION cm³
p	0.5	Zn	1.5x10^18
n	3	Se	7x10^17
n	.5	Se	8x10^18

GaAs CAP

Al₀.₉ Ga₀.₁ As

AR COATING

WINDOW (0.3 µm)

GaAs

SUBSTRATE

FABRICATION METHOD - MOCVD

Comparison of Solar Array
(Calculated Output)
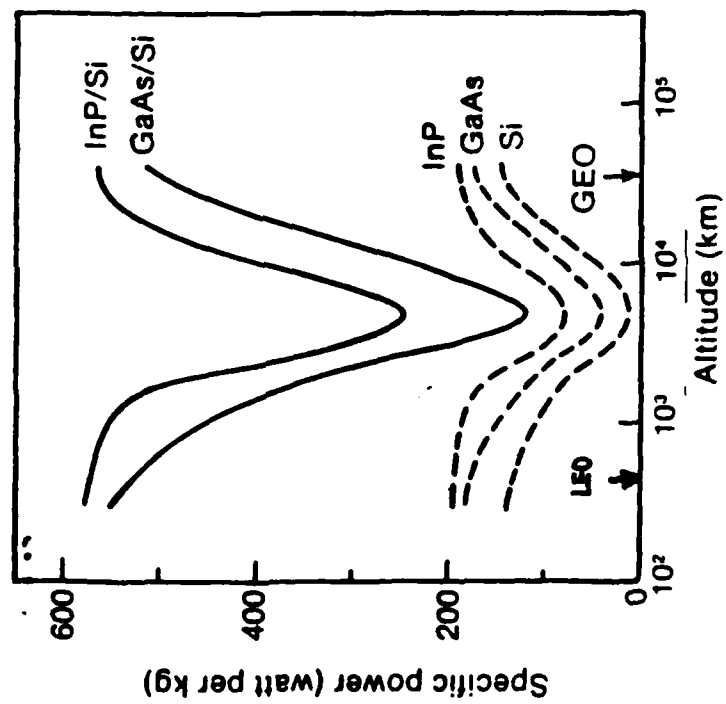
Solar Cell Radiation Damage
(InP Compared to GaAs and Si)

Electron
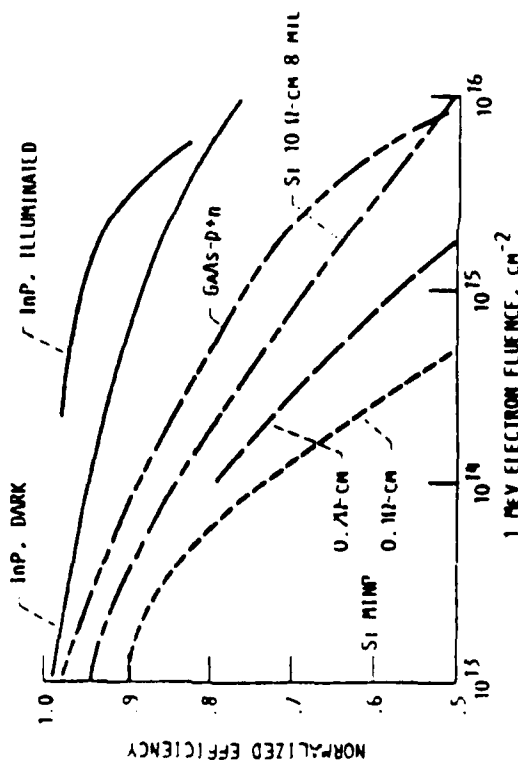
Gamma rays
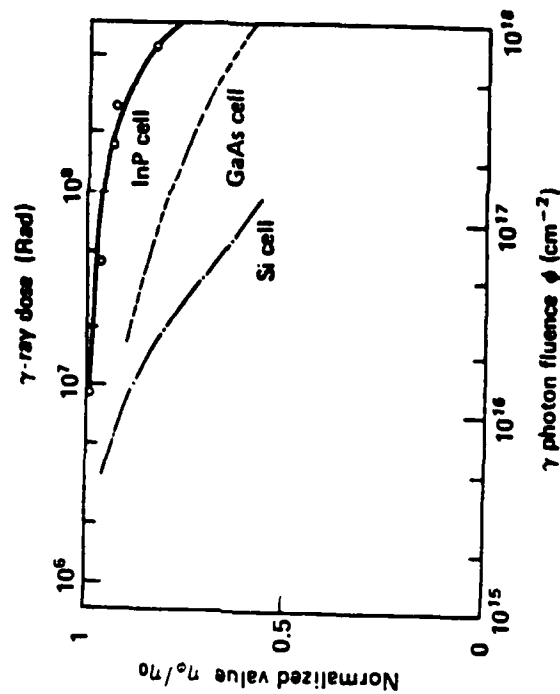
InP Solar Cell Thermal Annealing
(low temperature~100°C)

COMPLETE RECOVERY

1 MeV ELECTRON FLUENCE - 10^{17} cm^{-2}

TIME AT TEMPERATURE - 10 min

NORMALIZED MAXIMUM POWER

ANNEALING TEMPERATURE, °C
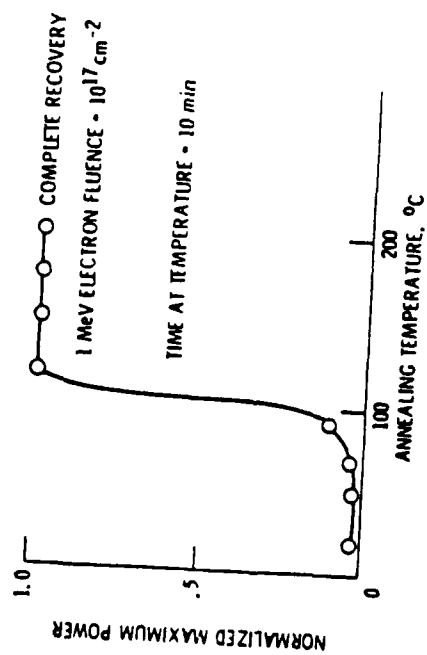
InP Solar Cells Concerns

- **Electron and Proton Damage**

    - Little difference between n+p and P+n cells
      (Electron-Normal Incidence Exp.)

    - Expect some difference between n+p and p+n cells for proton
      damage at both normal and omni directional situations
      (Refer to J. Y. Yaung and Sheng S. Li)

    - Further testing and numerical simulation are recommended.

Conclusion

* InP devices are normally harder than or equivalent to GaAs devices

* This assessment suggests InP device development for high hardness applications with strong *performance* requirement

Recommendations

- Device Simulations, device modelings, radiation effects modelings and radiation testings are recommended to ensure that performance/hardness will meet some special program requirements.

- Producibility enhancement factors should be considered early enough to reduce the cost.

  - programs (R&D) technical interchange
  - Isolate fundamental problems & resolve them by sharing resources

- Niche market exploration requires collaboration between system and the technology personnel

  - explore market opportunity
  - estimate/calculate payoffs carefully for technology insertion

2-40 GHz InGaAs HEMT MONOLITHIC DISTRIBUTED POWER AMPLIFIER

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H. Wieder*, and P. Chu*

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2-40 GHz InGaAs HEMT Monolithic Distributed Amplifier

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H. Wieder and P. Chu

University of California, San Diego
Department of Electrical and Computer Engineering
La Jolla, CA 92093

2 to 40 GHz InGaAs HEMT Monolithic Distributed Amplifier

TRW

CHIP SIZE = 0.8 × 1.0 mm²

23231289
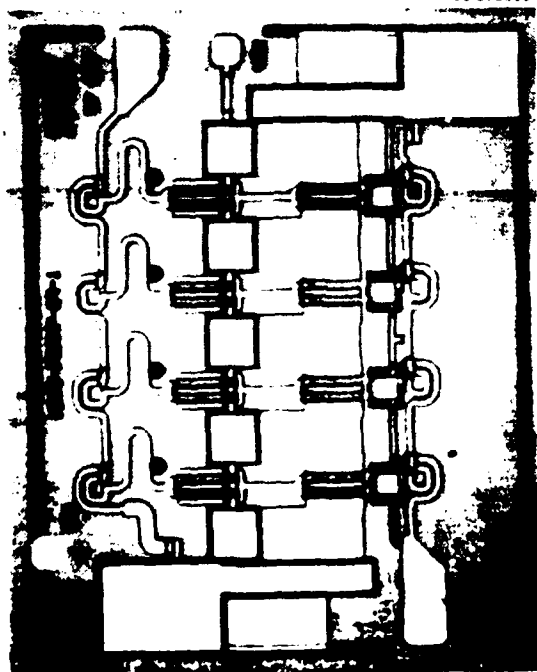
Performance

▲ >8 dB gain (2 to 35 GHz)

▲ >15 dBm P$_{-1}$ (20 GHz)

▲ 27 dBm IP$_3$(18 GHz)

Features

▲ 0.25 micron gate length

▲ 300 micron gate width

▲ Pseudomorphic InGaAs

▲ MIM capacitors

▲ Air bridges

▲ Source via grounds

GAIN (dB)

RETURN LOSS

FREQUENCY (GHz)

(dB)
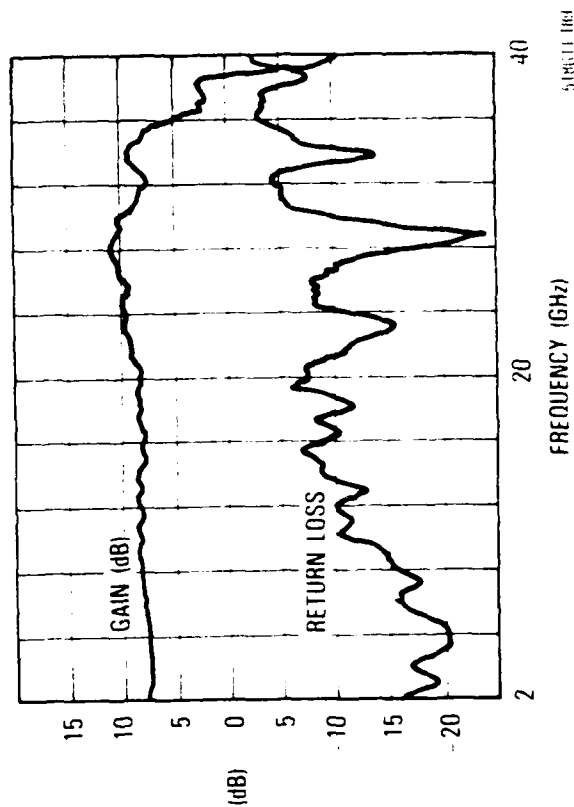
Comparison of Distributed Amplifier Performance

Performance \ Type	TRW AlGaAs/InGaAs	TRW AlGaAs/GaAs	Varian AlGaAs/GaAs
Bandwidth (GHz)	2 to 35	2 to 20	3 to 33
Gain (dB)	8	10	8
NF (dB)	N/A	3	3
P_{-1} (dBm)	15.4 (20 GHz)	N/A	13 (18 GHz)
IP_3 (dBm)	24.6 (20 GHz)	18	N/A

Conclusions

Pseudomorphic InGaAs HEMT provides significant performance advantages for wideband distributed amplifiers:

- Higher Gain

- Wider Bandwidth

- Higher Power Output

2 - 40 GHz InGaAs DISTRIBUTED POWER AMPLIFIER

M. LaCon   J. Yonaki   K. Nakano   K. Stolt   J. Berenz

TRW Inc.
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Abstract

This paper presents the design, fabrication and evaluation of a distributed wide-band mono-lithic amplifier using In-GaAs/GaAs pseudomorphic HEMTs. The measurement results show the amplifier operates from 2 to 40 GHz with 9.5 dB gain and 15 dBm P_{-1dB} output power. This is the best result reported for wide band distributed amplifiers, and the first cascode connected In-GaAs/GaAs HEMT distributed amplifier using constant R-networks for circuit matching. The amplifier chips developed are key components for EW applications. With our systematic design approach and In-GaAs/GaAs HEMT technology, development of ultra wide-band power amplifiers up to 100 GHz can be realized.

1 Introduction

The introduction of the traveling wave concepts has provided a new technique for wide-band amplifiers at millimeter wave frequencies. With the advent of In-GaAs/GaAs HEMTs, interest in a new class of wide-band amplifier circuits has increased. The distributed amplifier described here provides a method of achieving performance that is better than more conventional single gate FET circuits, and in a manner that allows the integration of larger periphery transistors suitable for high power amplification. In this paper, three techniques are used to address the problem of wide band power amplification: the use of constant-R networks rather than the more conventional constant-K network, the cascode connection of two transistors to augment a dual gate FET characteristic, and the use of a capacitive divider to overcome the higher input capacitance.

2 Design

The two principle advantages that make the InGaAs HEMT suitable for power amplification are high peak transconductance and high saturation currents. In this design, two transistors in each of 4 amplifier sections are cascaded together. The cascode configuration is facilitated by connecting a 300 micron common source HEMT in series with a common gate HEMT of the same source periphery. The two HEMTs are connected using a high impedance transmission line which can be used as a tuning element to correct the pass band response of the amplifier. The cascode connection of the two transistors provides several advantages[1, 2]. The drain bias is distributed across two transistors in each section of the amplifier. Since the bias voltage of each transistor is limited by the reverse breakdown of the gate to drain region, this configuration makes it possible to operate the power amplifier at higher bias voltages because the drain to source voltage is dissipated across

two transistors. The output impedance of the common gate HEMT is higher than the common source HEMT used at the input of each amplifier section. This provides a lower attenuation across the output matching network. The constant-R structure is realized using a folded coupled line connected with small parasitic transmission lines and an airbridge. The amplifier was designed by connecting the constant-R structures together with the parasitic input and output capacitances of the HEMT to form an artificial transmission line structure terminated in 50 ohms. The physical layout of the constant-R structure shown in Figure 1, presents a constant impedance which is independent of frequency. The coupled transmission line provides the mutual inductance and coupling capacitance, while the interconnecting transmission lines and airbridge crossover provide additional parasitic inductance and capacitance. A schematic representation of the constant-R network is shown in Figure 2. The advantage of this network over conventional constant-K networks can be seen in Figure 3. The result is a much higher cutoff frequency. The use of capacitive coupling is accomplished using thin film capacitors connected in series with the common source HEMTs of each amplifier section. The capacitors form a capacitive voltage divider at the gate terminal of each device reducing the magnitude of the input signal voltage[3]. When the capacitor is equal to the gate capacitance the equivalent input capacitance of each section of the amplifier is reduced by one half. The reduction in voltage across the gate capacitor results in a 3 dB drop in gain from each amplifier section. This can be compensated by doubling the source periphery, effectively doubling the power handling capability of the amplifier. A schematic of the distributed amplifier is shown in Figure 4.

To simulate and optimize the amplifier design, a non-linear model for the single gate HEMT is also derived. The characteristic of the non-linear elements in the linear model were determined using .25 X 300 micron In-GaAs/GaAs HEMT single gate device measurements at various bias conditions[4]. The non-linear simulation was performed by using time domain analysis.

3   Fabrication

The circuit was fabricated on an In-GaAs/GaAs heterostructure wafer grown with MBE. The device structure in Figure 5 utilizes a TRW baseline planar HEMT process.

The process begins with oxygen ion implantation to obtain device isolation. This implantation process is critical for uniform EBL gate processing. Ohmic contacts are deposited using gold-germanium metalization. A contact resistance of less than .08 ohm-MM is achieved by using rapid thermal alloying. Thin film resistors (ni-chrome) are deposited by a standard liftoff process for the bias networks and distributed network terminations. A thin layer of metal (Ti-Au) is deposited to form the first level metal; this layer is used to form the matching networks and bottom plate of the capacitors. Electron beam lithography is used to define the .2 to .25 uM gate length resist patterns. Gate recess etching is performed followed by gate metal deposition. A thin dielectric film (silicon-dioxide) is deposited to form the MIM capacitors. The capacitors are used in DC blocking and RF bi-passing functions. The top metal is defined using an airbridge process. This form of interconnection reduces crossover parasitics and improves circuit yield. Liftoff techniques are used in both dielectric and top metal process steps. The substrate thickness is reduced by lapping the wafer to .1 MM. The substrate vias and backside metalization complete the process. The distributed amplifier chip is illustrated in Figure 6. The chip measures .85 X 1.5 MM and contains eight .25 X 300 uM cascode connected single gate HEMTs.

4 Results

A comparison of non-linear simulation and measured results shows good agreement. A plot of the measured and simulated results is shown in Figure 7. The amplifier has a measured gain of 9.5 dB. The close match not only verifies our model but also ensures that the design approach developed can be extended to higher frequencies. The saturation characteristics are shown in Figure 8, the amplifier exibited a 15.35 dBm P_{-1dB} compression point.

5 Conclusion

A compact wide-band power amplifier has been described in which InGaAs/GaAs HEMTs exhibit high gain-bandwidth product, high power output, and excellent linearity. Based on the size of the chip and the performance, this circuit will be a very attractive candidate for many wide-band amplifier applications.

6 Acknowledgments

The authors would like to express their gratitude to the people who helped make the results of this paper possible: Po-Hsin Liu, An-Chin Han, Susan Hertweck, Linda Klamecki, Rosie Dia, and Laurie DeLuca.

References

[1] E. M. Chase and W. Kennan, "A Power Distributed Amplifier Using Constant-R Networks," IEEE International Monolithic Circuits Symposium, IMCS-12, June 1986.

[2] E. Ginzton, W. Hewlett, J. Jasberg and J. Noe, "Distributed Amplification," Proc. IRE., August 1948.

[3] Y. Ayasli, L. Reynolds, R. Mozzi, and L. Hanes, "Capacitively Coupled Traveling-Wave Power Amplifier," IEEE International Monolithic Circuits Symposium, June 1984.

[4] M. LaCon, K. Nakano, and G. S. Dow, "A Wide Band Distributed Dual Gate HEMT Mixer," IEEE International Monolithic Circuits Symposium, November 1988.
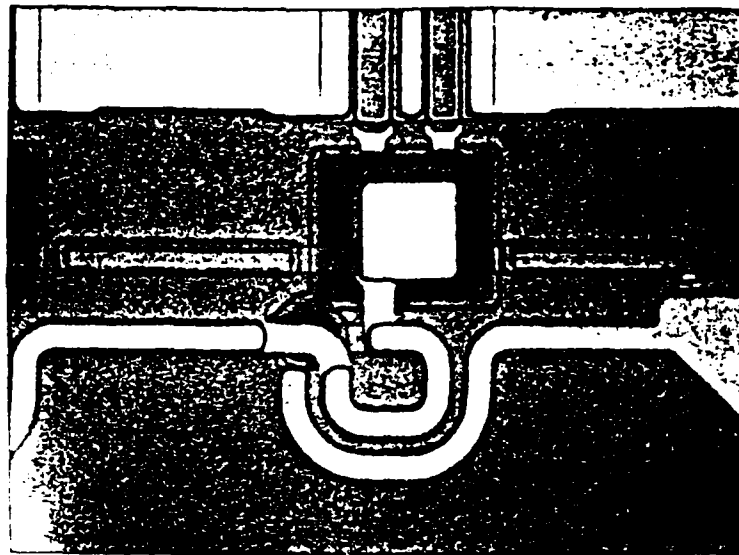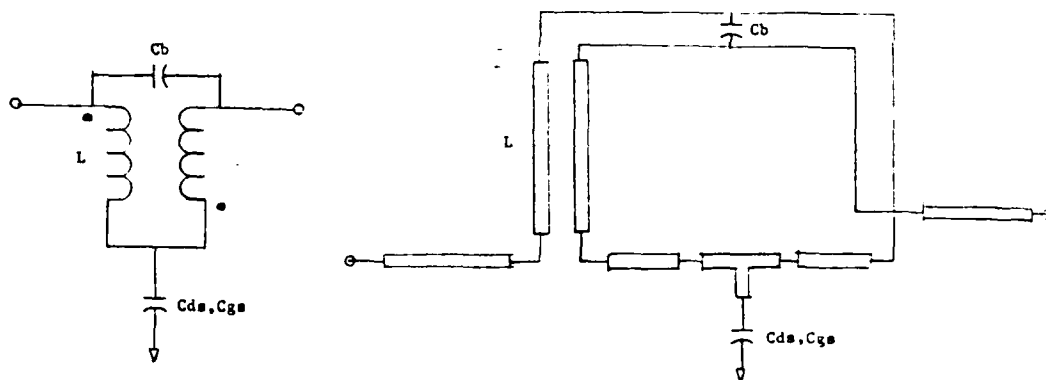
Figure 1: Constant-R Structure.

Figure 2: Schematic of Equivalent Circuit For Constant-R Structure.
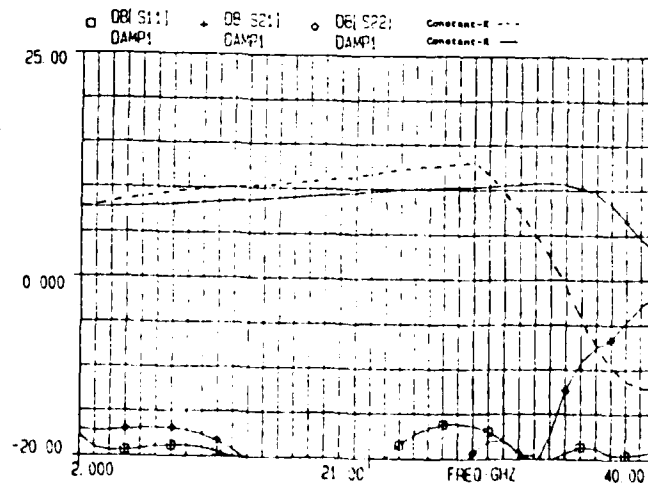

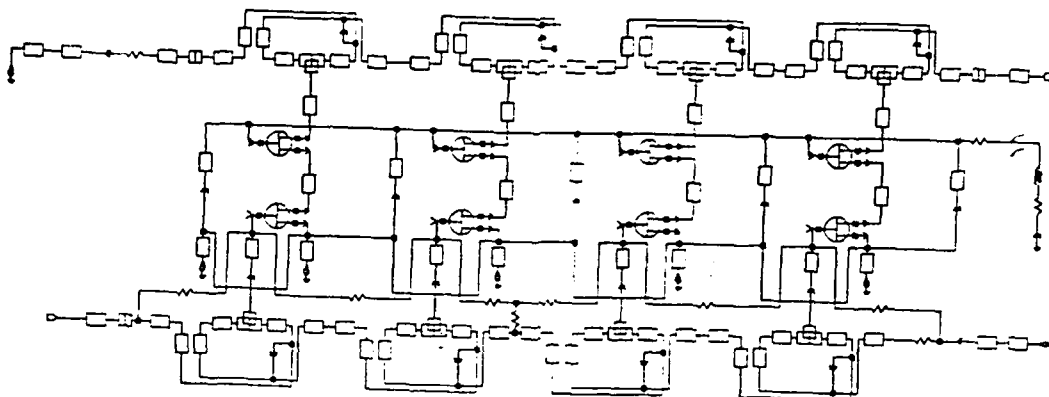Figure 3: Performance Comparason of Constant-K And Constant-R Networks.

Figure 4: Schematic of Distributed Power Amplifier.

| 500Å Si-doped n+ GaAs |
| 25Å undoped GaAs "spacer" |
| 300Å undoped InGaAs (15% In) |
| 0.5 μ undoped GaAs buffer |
| undoped LEC GaAs substrate |

Figure 5: In-GaAs/GaAs HEMT Device Structure.
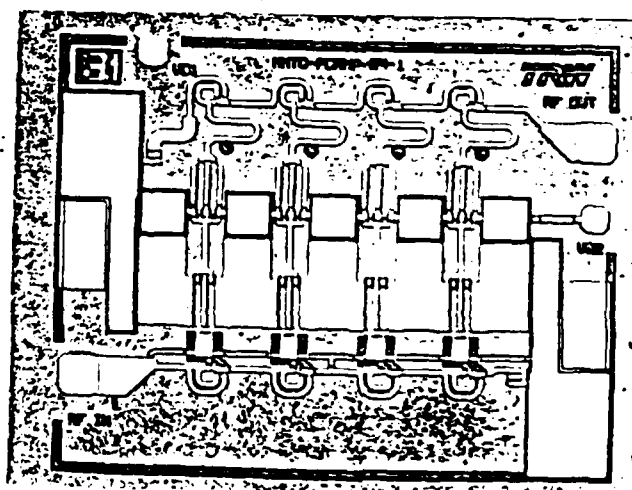
Figure 6: Photograph of Distributed Power Amplifier Chip.

CURSOR

1: -7.60 dB
2: +8.29 dB

dB

Vd=4.5V
Vgs1=-.21V
Vgs2=1.3V
Ids=142mA

Measured ——
Modeled   ---
Pin=-10dBm

2GHz   40GHz

401 points
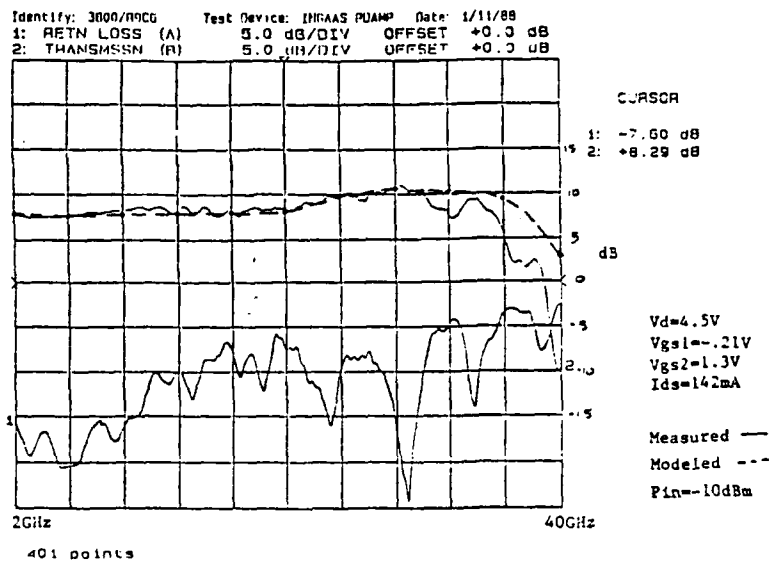
Figure 7: Comparison of Measured vs Simulated Performance.

WAFER 3800 R9C5 InGaAs POAMP
5.5V/147mA

1dB COMPRESSION PT.
15.35dBm

20 GHz

POWER OUT (dBm)

POWER IN (dBm)
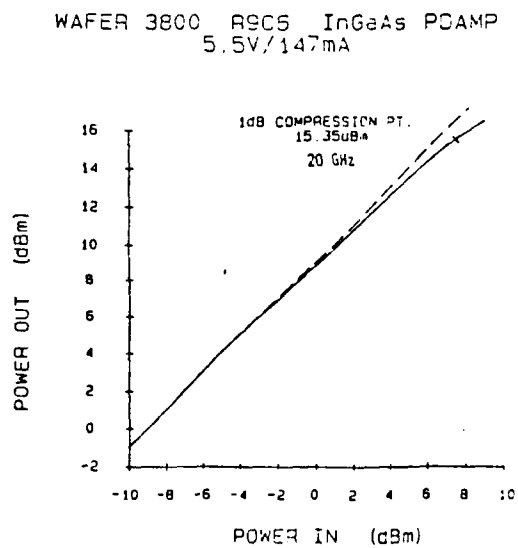
Figure 8: Distributed Amplifier P_{-1dB} Compression Point.

HIGH EFFICIENCY, WIDEBAND GaInAs MISFET AMPLIFIERS

D. Bechtle, P. D. Gardner and S. Y. Narayan

David Sarnoff Research Center
Subsidiary of SRI International
Princeton, NJ

HIGH EFFICIENCY, WIDEBAND GaInAs MISFET AMPLIFIERS

by

D. BECHTLE, P. D. GARDNER, AND S. Y. NARAYAN

DAVID SARNOFF RESEARCH CENTER
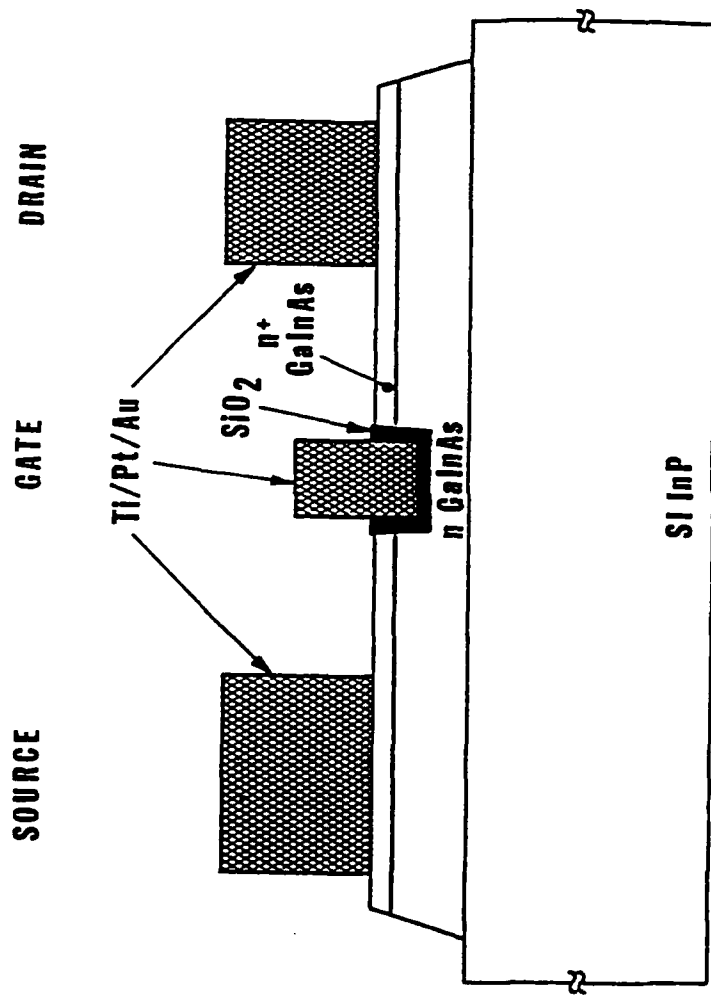## SUBSIDIARY SRI INTERNATIONAL

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INTRODUCTION

WE HAVE DEVELOPED n-CHANNEL, DEPLETION-MODE GaInAs MISFET TECHNOLOGY TO DEMONSTRATE THE POTENTIAL OF THIS MATERIAL FOR MICROWAVE POWER AMPLIFIER APPLICATIONS.

HIGHLIGHTS INCLUDE:

- SELF-ALIGNED-GATE PROCESS DEVELOPED

- FIELD EFFECT MOBILITY AS HIGH AS 7200 cm²/Vs DEMONSTRATED (FATFET)

- CARRIER VELOCITY OF 4×10^7 cm/s DEMONSTRATED FOR 0.7 μm GATELENGTH MISFET (FROM I-V CHARACTERISTICS)

- EXCELLENT MICROWAVE PERFORMANCE FOR 1-μm-GATELENGTH MISFETs
  - F_{max} ~ 65 GHz (FROM S-PARAMETERS)
  - 54% POWER-ADDED-EFFICIENCY AT 12 GHz (0.57 W/mm)
  - 32% POWER-ADDED-EFFICIENCY AT 20 GHz (0.43 W/mm)
  - 114 mW POWER OUTPUT AT 32.5 GHz

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SCHEMATIC CROSS-SECTION OF GaInAs MISFET

Top View

Gate Circuit

Drain Circuit

GaInAs MISFET

.125 mm Alumina

Side View

GaInAs MISFET

Drain Lead

Gate Lead

Source Pad

Thermkon Pallet
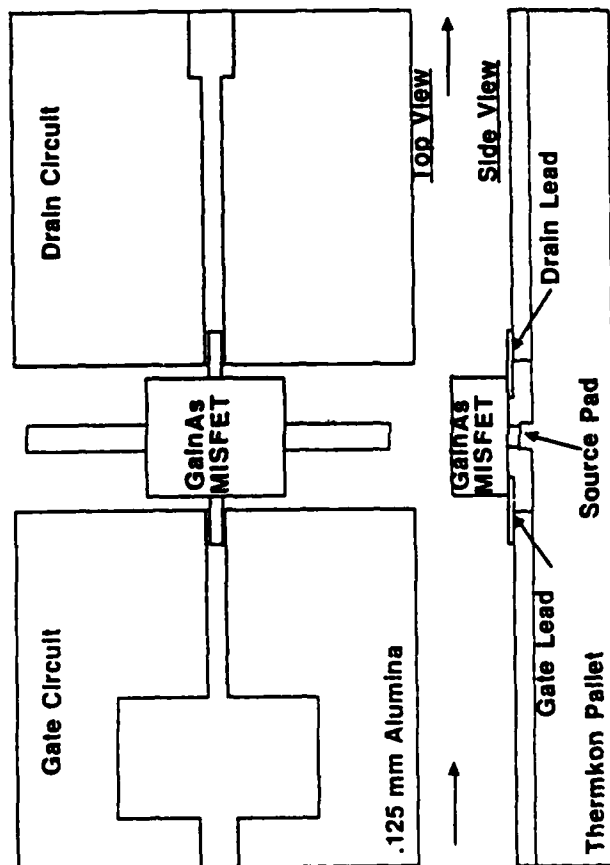
GaInAs MISFET WIDE-BAND AMPLIFIER
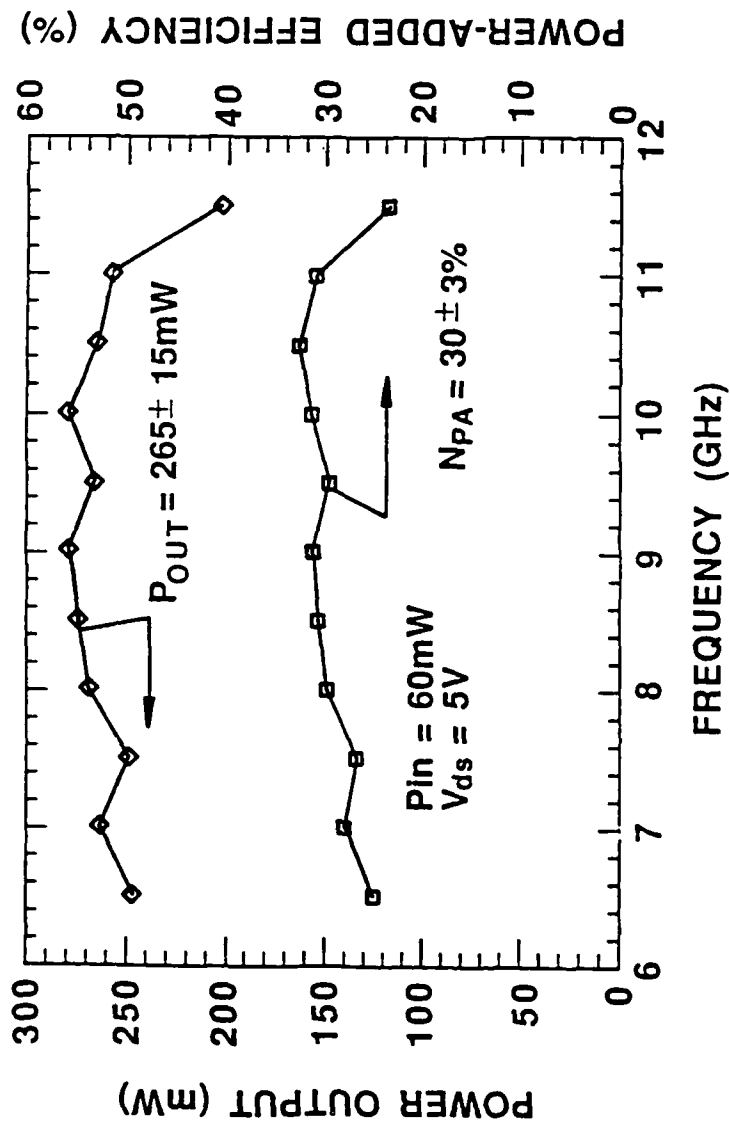
GaInAs MISFET AMPLIFIER 7-11 GHz PERFORMANCE-TUNED
FOR MAX POWER OUTPUT
(Gatelength 1 μm, Gatewidth 0.56 mm)
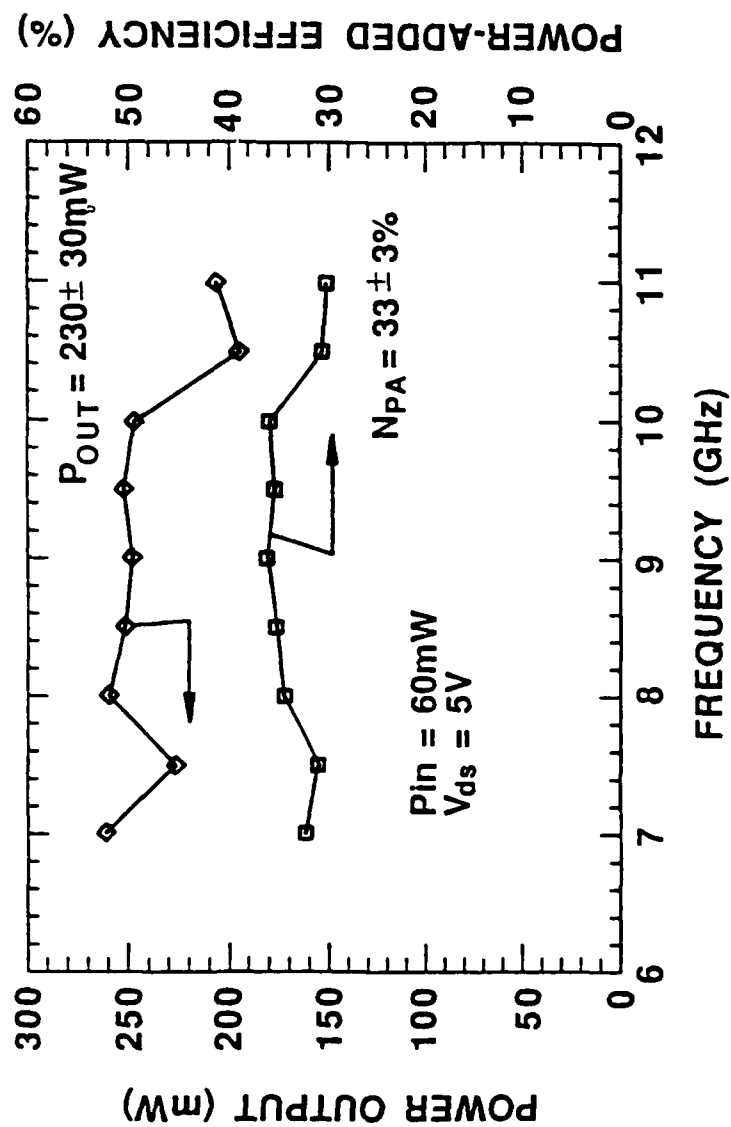
GaInAs MISFET AMPLIFIER 7-11 GHz PERFORMANCE-TUNED FOR MAX EFFICIENCY
(Gatelength 1 μm, Gatewidth 0.56 mm)

POWER-ADDED EFFICIENCY (%)

POWER OUTPUT (mW)

FREQUENCY (GHz)

$P_{OUT} = 220 \pm 85mW$

$N_{PA} = 29 \pm 4\%$

Pin = 60mW
V_{ds} = 4.5V
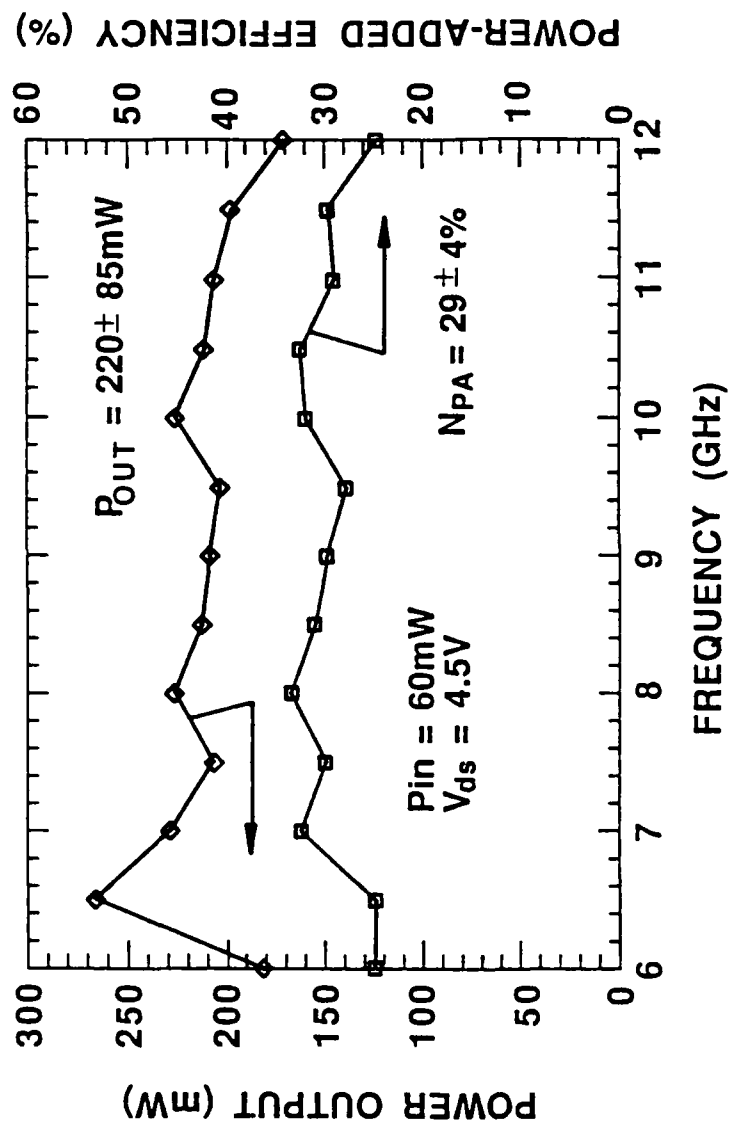
GaInAs MISFET AMPLIFIER 6-12 GHz PERFORMANCE
(Gatelength 1 μm, Gatewidth 0.56 mm)
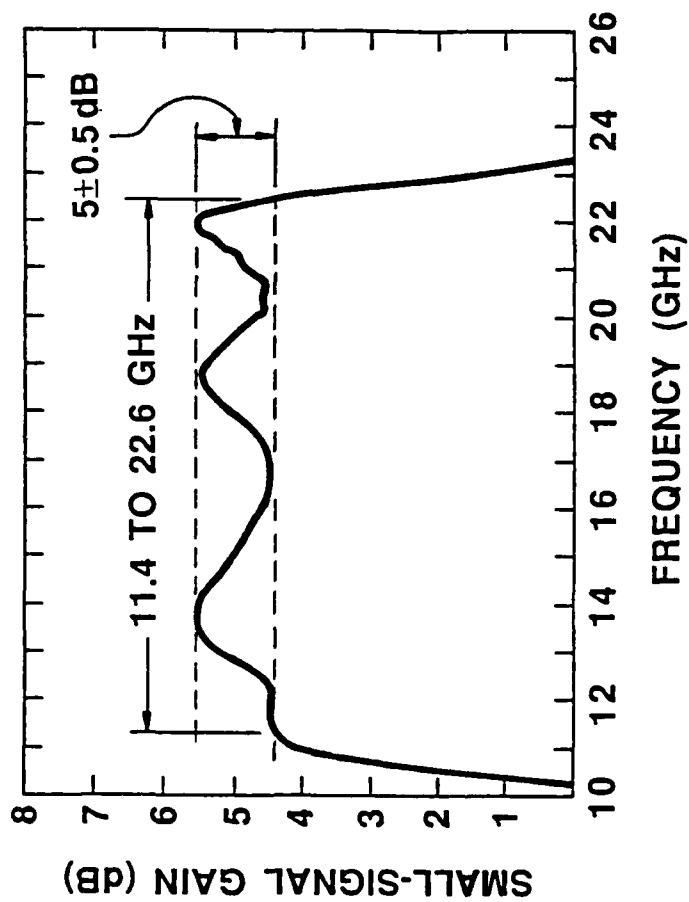
GaInAs SMALL-SIGNAL AMPLIFIER PERFORMANCE
(Gatelength 0.7 μm, Gatewidth 0.56 mm)

SUMMARY & CONCLUSIONS

GaInAs MISFETs PROVIDE

- HIGH OPERATING FREQUENCY

  - SUPERIOR SEMI-CONDUCTING PROPERTIES

- HIGH POWER-ADDED EFFICIENCY & POWER OUTPUT

  - SUPERIOR SEMI-CONDUCTING PROPERTIES

  - MISFET STRUCTURE

- HIGH EFFICIENCY WIDEBAND AMPLIFIER PERFORMANCE IN SIMPLE MICROWAVE CIRCUITS

  - 230 mW OUTPUT POWER WITH 33% POWER-ADDED EFFICIENCY OBTAINED OVER 7 TO 11 GHz BAND USING A SINGLE 0.56 mm GATEWIDTH, 1 μm GATELENGTH GaInAs MISFET

  - SMALL SIGNAL 11.4 TO 22.6 GHz BANDWIDTH OBTAINED USING 0.7 μm GATELENGTH, 0.56 mm GATEWIDTH GaInAs MISFET

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NOVEL APPLICATIONS OF InP BASED TECHNOLOGY: NEUROCOMPUTING

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HIGH T_c
SUPERCONDUCTING MATERIALS

- Only applications that are revolutionary rather than evolutionary will find market place immediately.

- Typical Example: Neurocomputing

NEUROCOMPUTING:

Deals with non–programmed adaptive information processing systems (neural network)

NEURAL NET:

A neural network consists of a collection of computational units (neurons) that models some of functionality of the human nervous systems and attempts to capture some of its computational strength.

DIGITAL Vs. ANALOG

A–Digital

Strengths

- Design techniques are advanced.
- Noise immunity is high.
- Computational speed can be very high.
- Learning networks can be implemented readily.

Weaknesses

- Digital circuits must be synchronous while real neural nets are asynchronous.
- All states in a digital network are quantized.

B–ANALOG

Strengths

- Asynchronous behavior is automatic.
- Smooth neural activation is automatic.
- Circuit elements can be small.

Weaknesses

- Noise immunity is low.
- High precision is not possible.
- No reliable analog, nonvolatile memory technology exist.

STRATEGY FOR NEW PRODUCT DEVELOPMENT

- Analyze the state of the art.

- Propose new schemes which build on any strengths and/or remove any limitations that are revealed by the analysis.

```
┌─────────────────────────┐
│   Discovery of High     │
│ Temp. Superconducting   │
│      Phenomena          │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐
│    Development of        │
│  Thin Film Deposition    │
│      Techniques          │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐
│    Development of        │
│   Devices Suitable       │
│  For DSP Applications    │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐
│    Fabrication of        │
│  Superconducting Chip    │
│   Based on Available     │
│     Architecture         │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐
│     Compete with         │
│ Advanced Semiconductor   │
│    Digital Signal        │
│      Processor           │
└─────────────────────────┘
            │
            ▼
┌─────────────────────────┐
│   Low Probability of     │
│   Market Penetration     │
└─────────────────────────┘
```
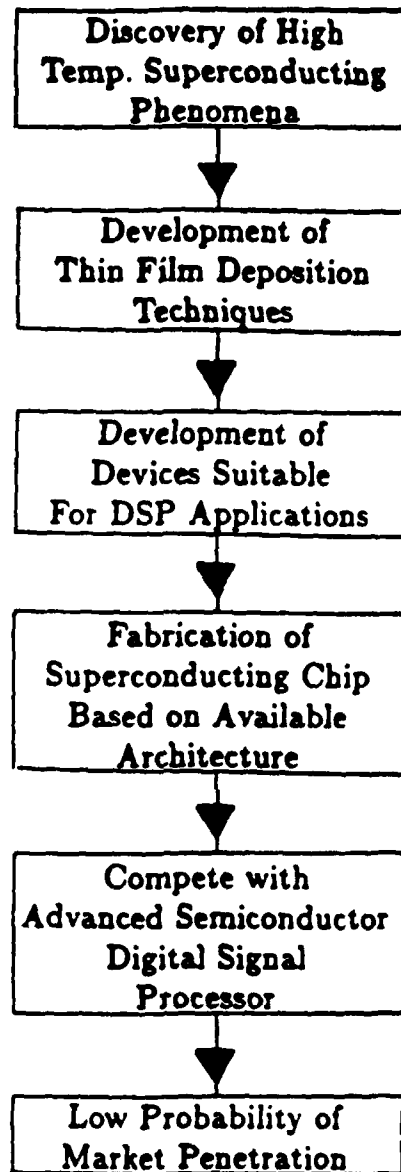
EVOLUTIONARY APPROACH

Fig. 2. Evolutionary scheme for the realization of advanced signal processor.

429
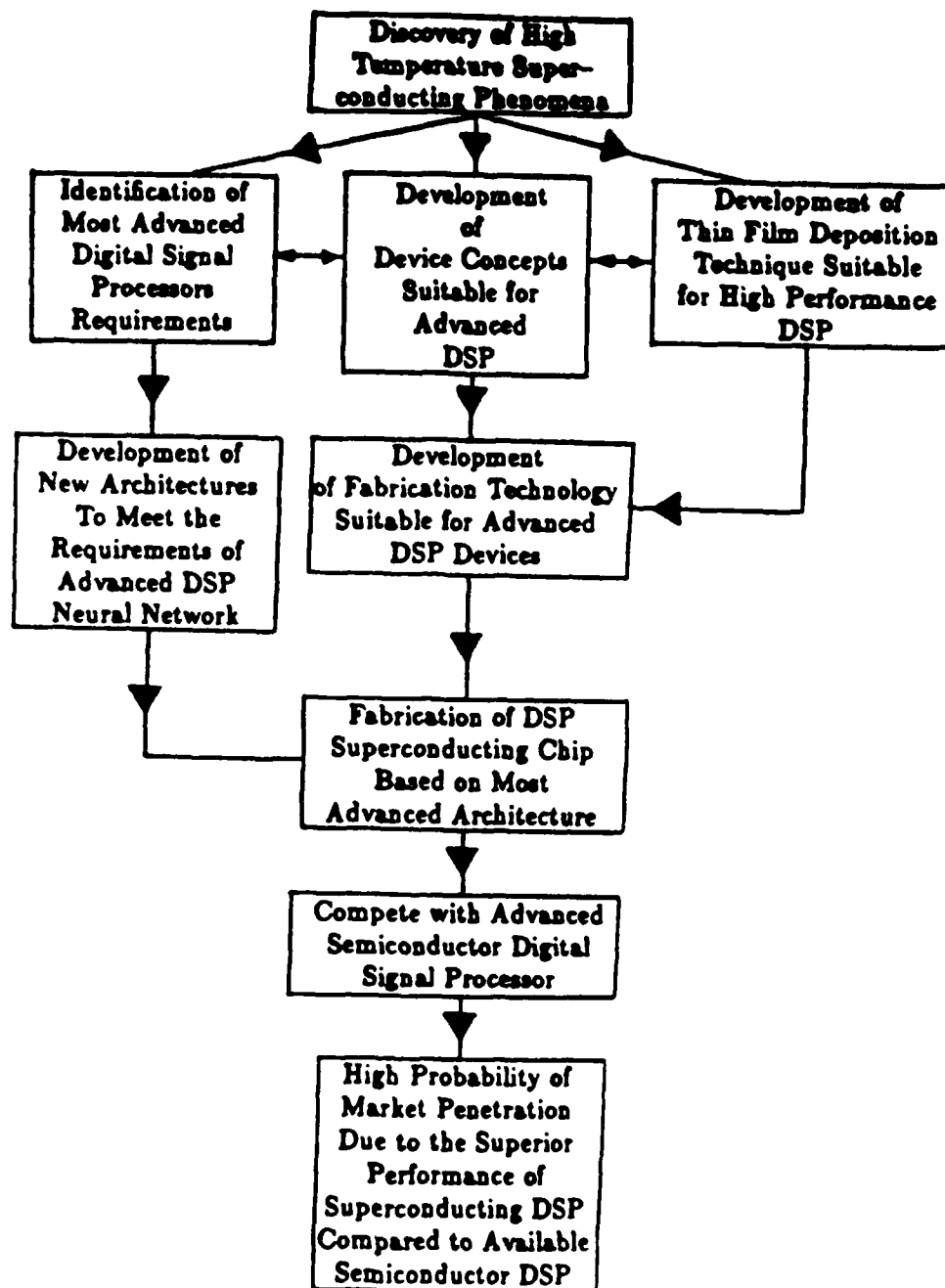
REVOLUTIONARY APPROACH

Fig. 3. Revolutionary scheme for the realization of advanced signal processor.

Superconductor vs. Semiconductor Electronics

Superconducting Electronic Devices

Advantages:
1. High Speed
2. Ultra Low Power
3. High Speed Interconnects

Limitations:
1. Limited Integration Density
2. Non-Transistor-like Devices
   Latching (must be reset)
   Use threshold (not restoring) logic
   Non-Inverting
3. Low (if any) Power Gain

Semiconductor Electronic Devices

Advantages:
1. High Integration Density
2. Transistor Properties
3. High Power Gain

Limitations:
1. High Power Dissipation Density
2. Significant Interconnect Delay

(note complementarity of technologies)

Hybrid Electronics:

An Anti-Traditional Technology

Results of High Temperature Superconductor Developments

1. Conventional superconducting devices still have the same limitations

2. Overlap of allowable operating temperatures for superconductor and semiconductor electronics

Hybrid devices and systems are now feasble

Why Develop Hybrid Superconductor/Semiconductor Devices?

1. The complimentary advantages of the two technologies would combine, rather than compete

2. Improvements of hybrid systems would result from advances in either technology

Hybrid Device Considerations

Desired characteristics of hybrid devices

    1. Include essential structures and operating mechanisms of semiconductor devices

    2. Incorporate superconductors and superconducting phenomena to improve operation

Types of hybridized semiconductor devices

    1. Passive hybrid - superconducting interconnects

    2. Active hybrid - operating mechanisms modified by inclusion of superconductors

Fabrication Concerns

    1. Device integrity must be maintained through all phases of fabrication

    2. Acceptable superconductor/semiconductor interfaces must be attainable and stable

Hybrid System Contact Configurations

Superconducting Interconnect
Semiconductor Device

Direct Contact Interface

Superconducting Interconnect
Metal Interface
Semiconductor Device

Metal Intermediary Interface
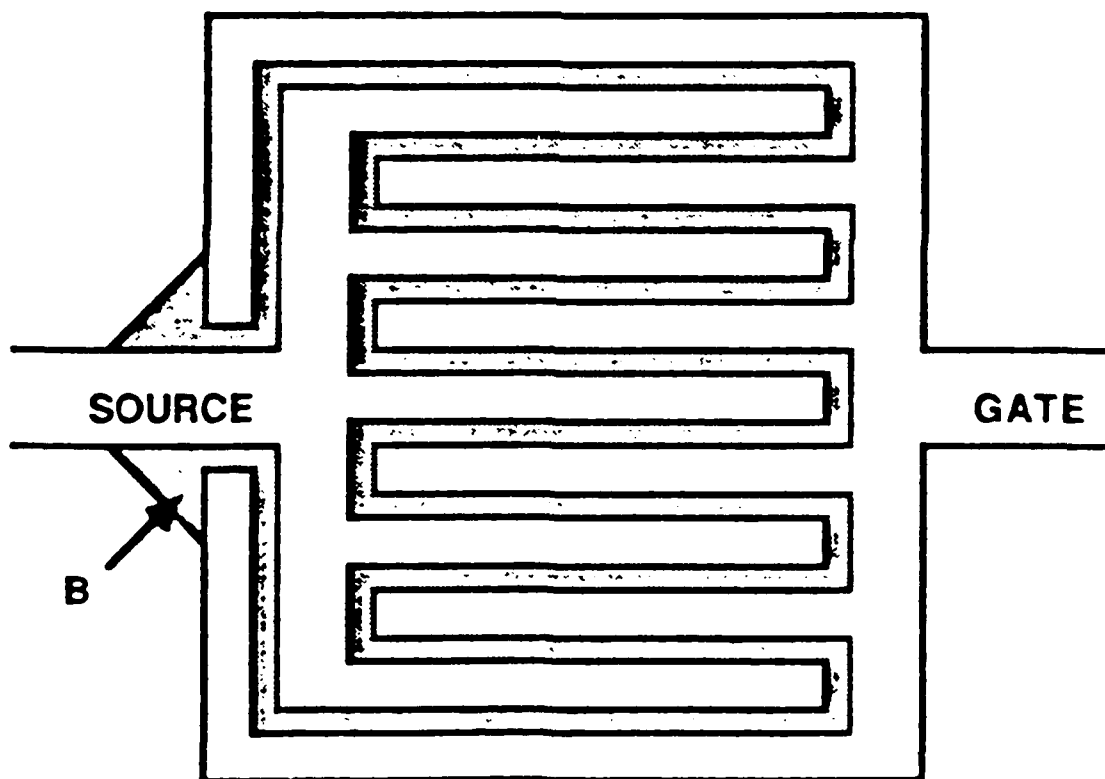
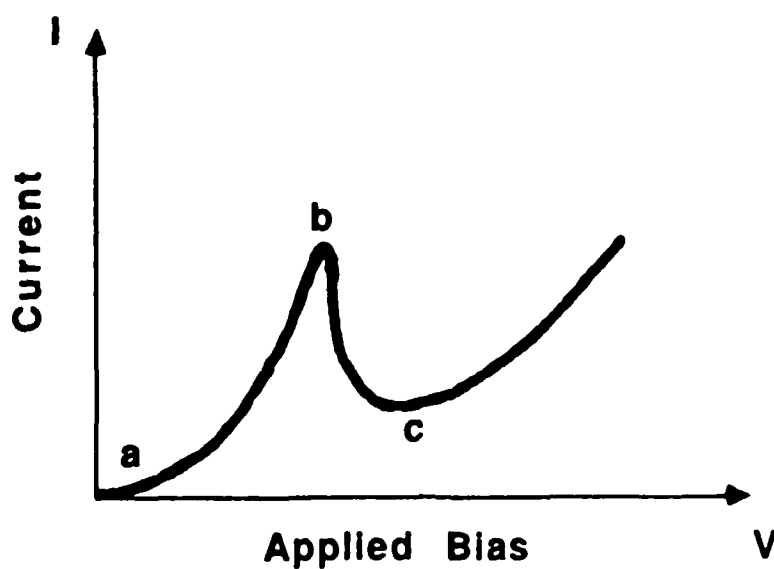| Superconducting Interconnect |
|---|
| Dielectric Barrier |
| Semiconductor Device |

Protective Barrier Interface
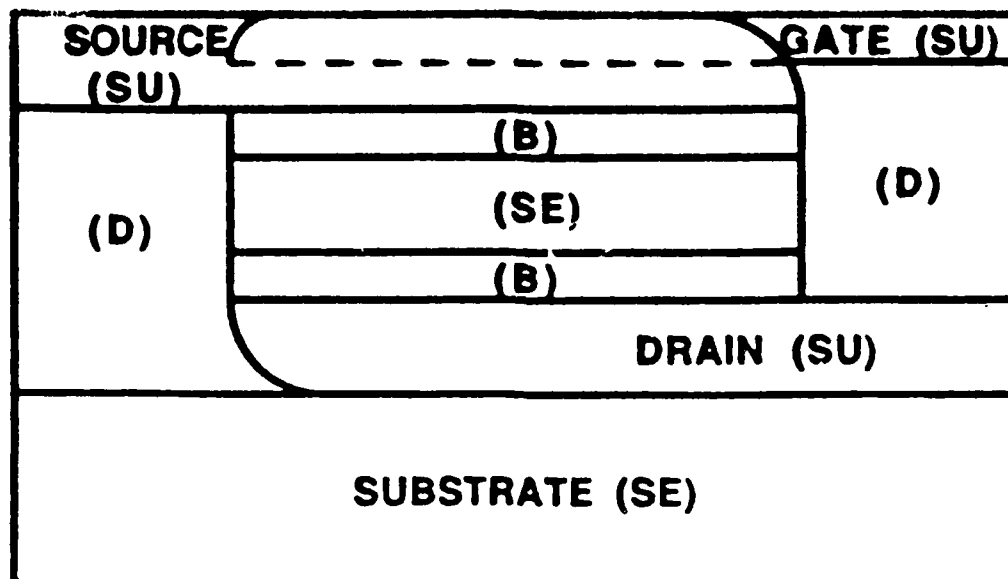
RTT Side View

Source/Gate Configuration

SU: Superconductor SE: Semiconductor
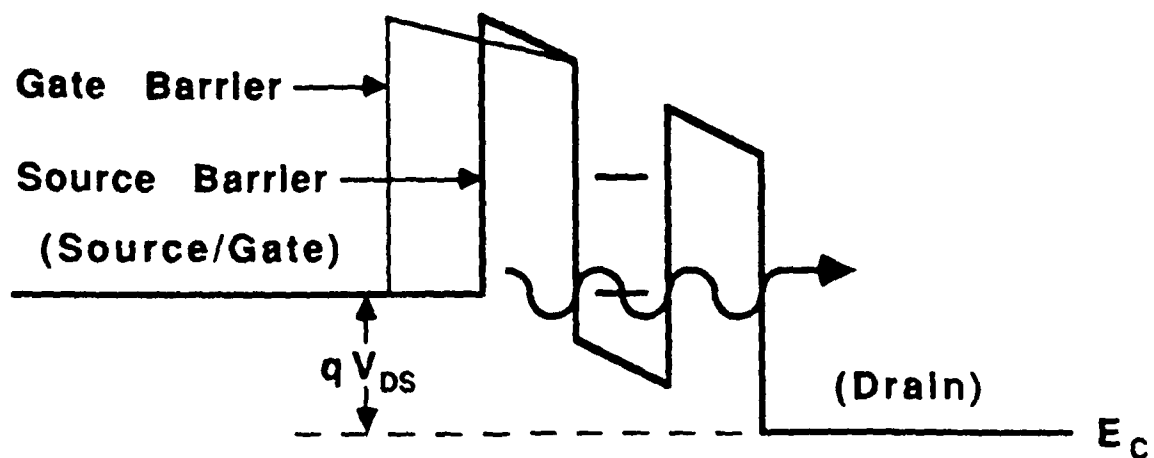B: Barrier Layer D: Dielectric

Proposed Hybrid RTT Structure
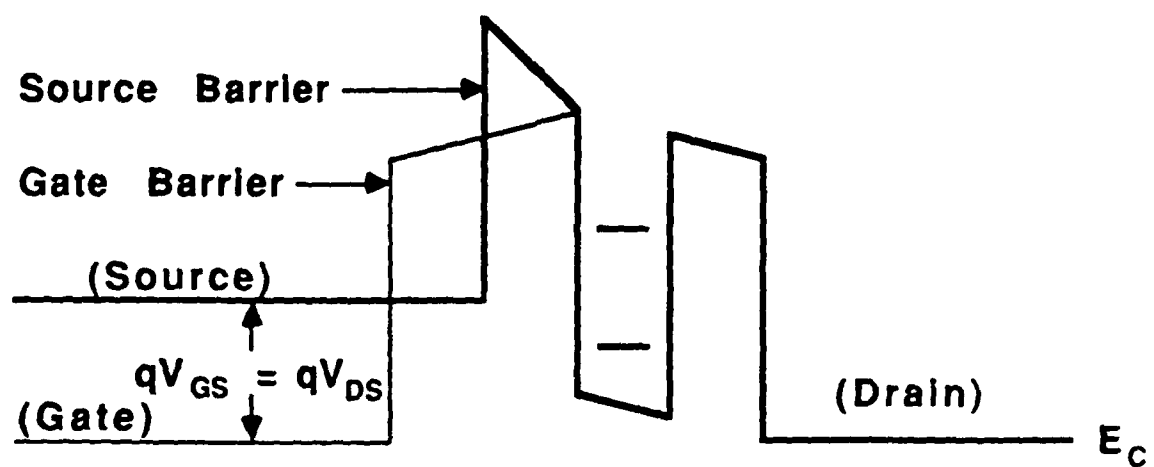
a) Unbiased   b) Resonance

c) Anti-Resonance

C: Cathode

A: Anode
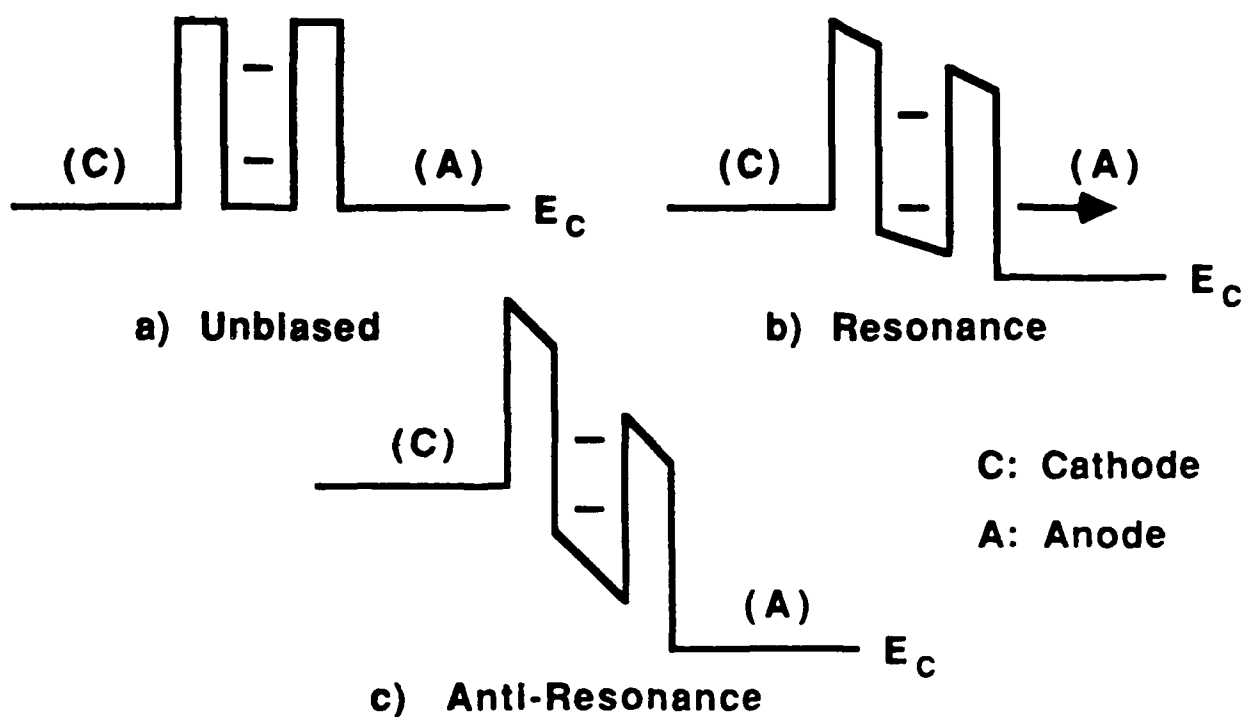
Resonant Tunnel Diode Conduction Band Diagrams

Resonant Tunnel Diode I-V Characteristic

Gate Barrier →

Source Barrier →

(Source/Gate)

qV_{DS}

(Drain)

E_C

$V_{GS} = 0$ (Resonance)

Source Barrier →

Gate Barrier →

(Source)

$qV_{GS} = qV_{DS}$

(Gate)

(Drain)

E_C

$V_{GS} = V_{DS}$ (Anti-Resonance)

RTT Conduction Band Diagrams
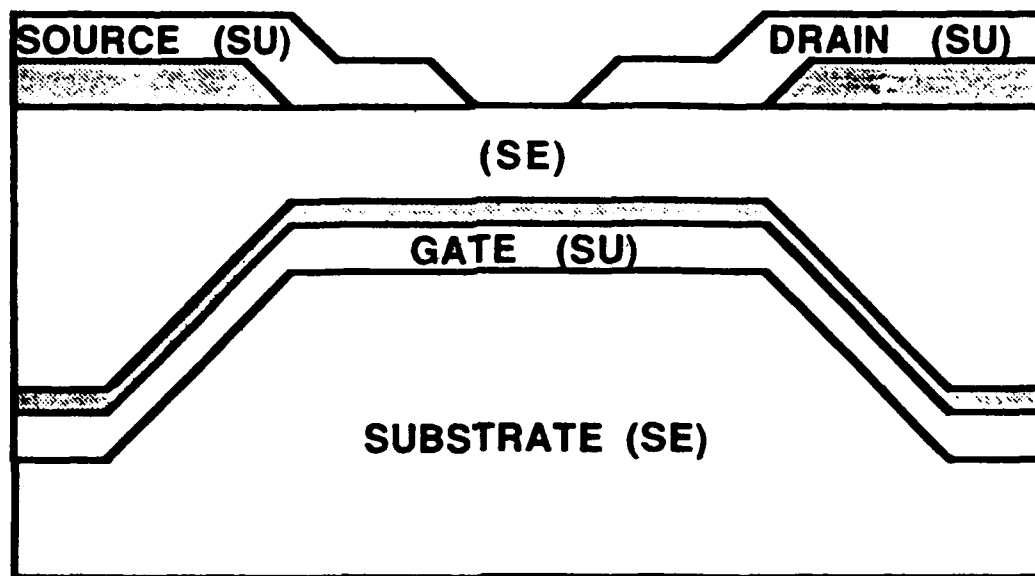
SU: Superconductor   SE: Semiconductor

Dielectric

Hybrid MOSFET Device Structure

Conclusions about Characteristics of Next-Generation Devices

Characteristic	Reasons
1. Quantum Controlled	No suppression or ignoring of wave nature of matter
	More efficient operation (only fundamental limits)
2. Heterojunctions	Abrupt, not gradual
	Don't degrade with scaling
	Allow thinner active region
	Band gap engineering
3. Vertical Structure	Less variability of dimensions
	Thinner active region
	Higher current capability

Desired Result: sub-picosecond switching

Proposals: 1.   The Resonant Tunneling Transistor

2.   Superconductor/Semiconductor Hybrids

OUR PROPOSED DEVICES BASICALLY VERTICAL STRUCTURES

$$L = 0.1 \mu m$$

$$W = 1 - 10 \mu m$$

$$\text{AREA} = 0.1 - 1.0 \mu m^2$$

SWITCHING SPEED $\simeq 10 - 100 fs (1 fs = 10^{-15} \text{s})$
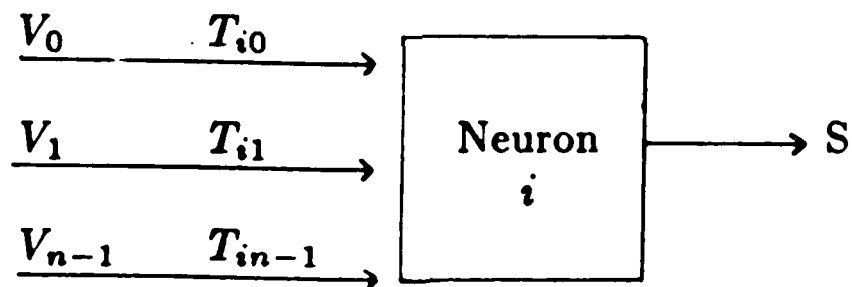
ULTRAFAST, AND ULTRA DENSE PACKAGING.
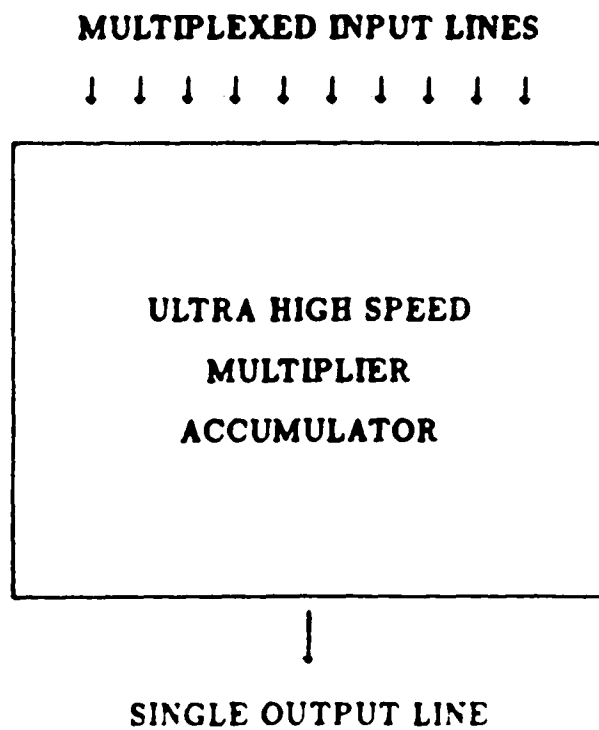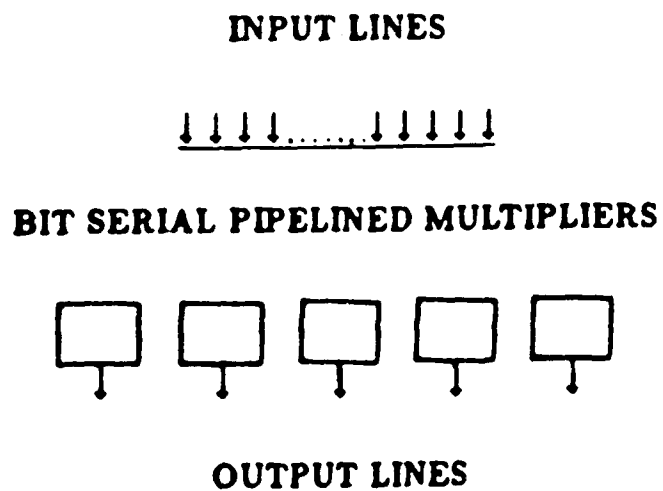
KEY MATHEMATICAL EXPRESSION:

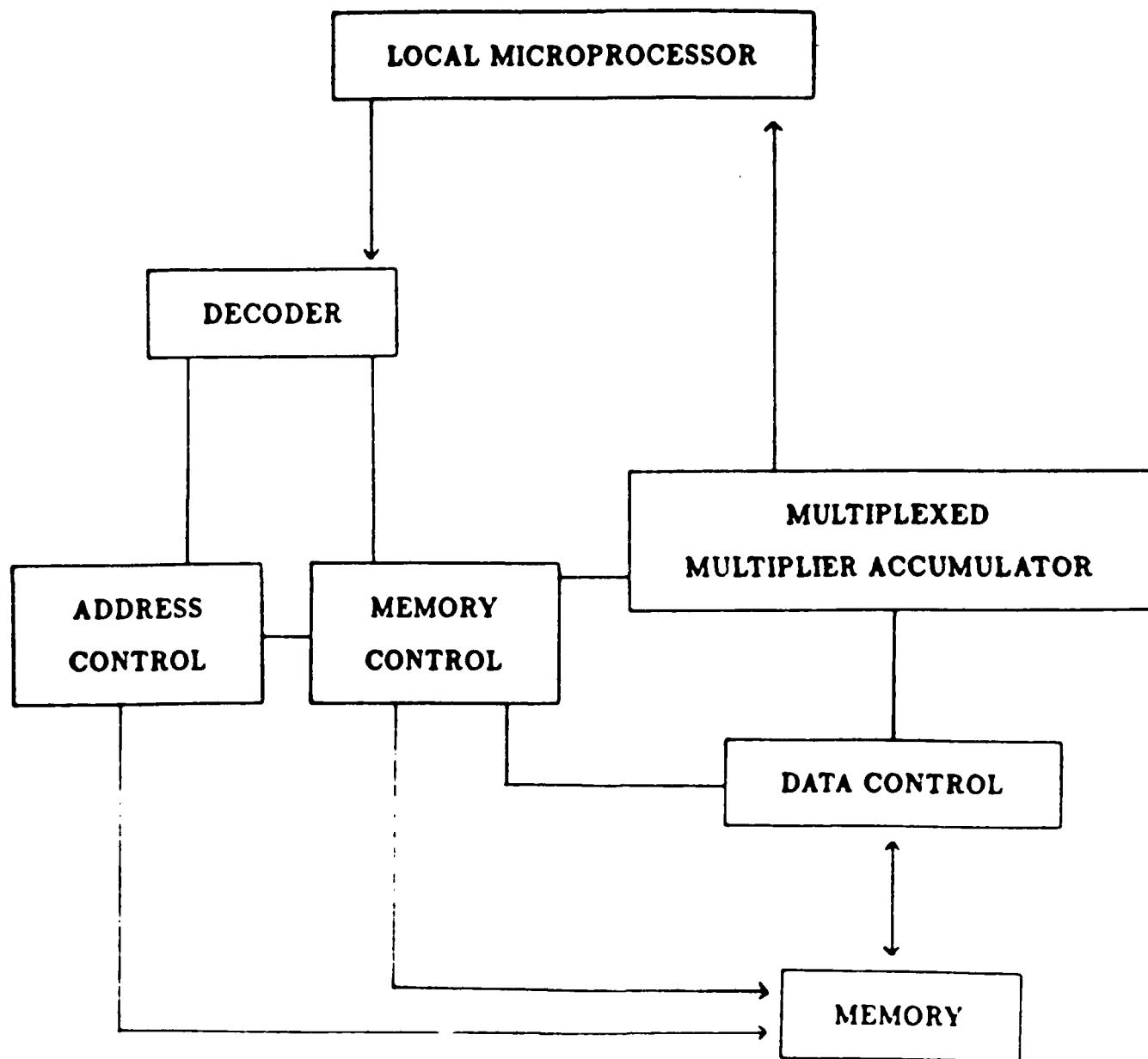$$S = \sum_{j=0}^{n-1} T_{ij} V_j$$

n = number of neurons in the neural network

V_j = state of neuron j

T_{ij} = synaptic weight of the neuron i related to input V_j

MULTIPLEXED INPUT LINES

↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓

INPUT LINES

↓↓↓↓......↓↓↓↓↓

BIT SERIAL PIPELINED MULTIPLIERS

ULTRA HIGH SPEED

MULTIPLIER

ACCUMULATOR

OUTPUT LINES

↓

SINGLE OUTPUT LINE

442

PERFORMANCE AVALUATION

Chip Area

The resonant tunneling transistor, because of its vertical structure, has no device area beyond its contacts. For an 8 x 8 bit parallel multiplier the required chip area will be
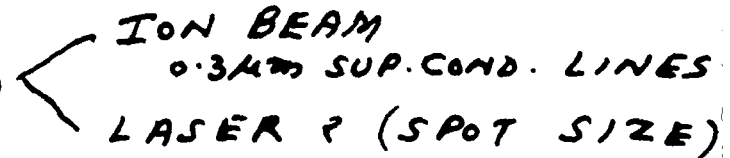
$$\text{RTT Realization} \approx 0.7mm^2$$

$$\text{CMOS Realization} \approx 2.0mm^2$$
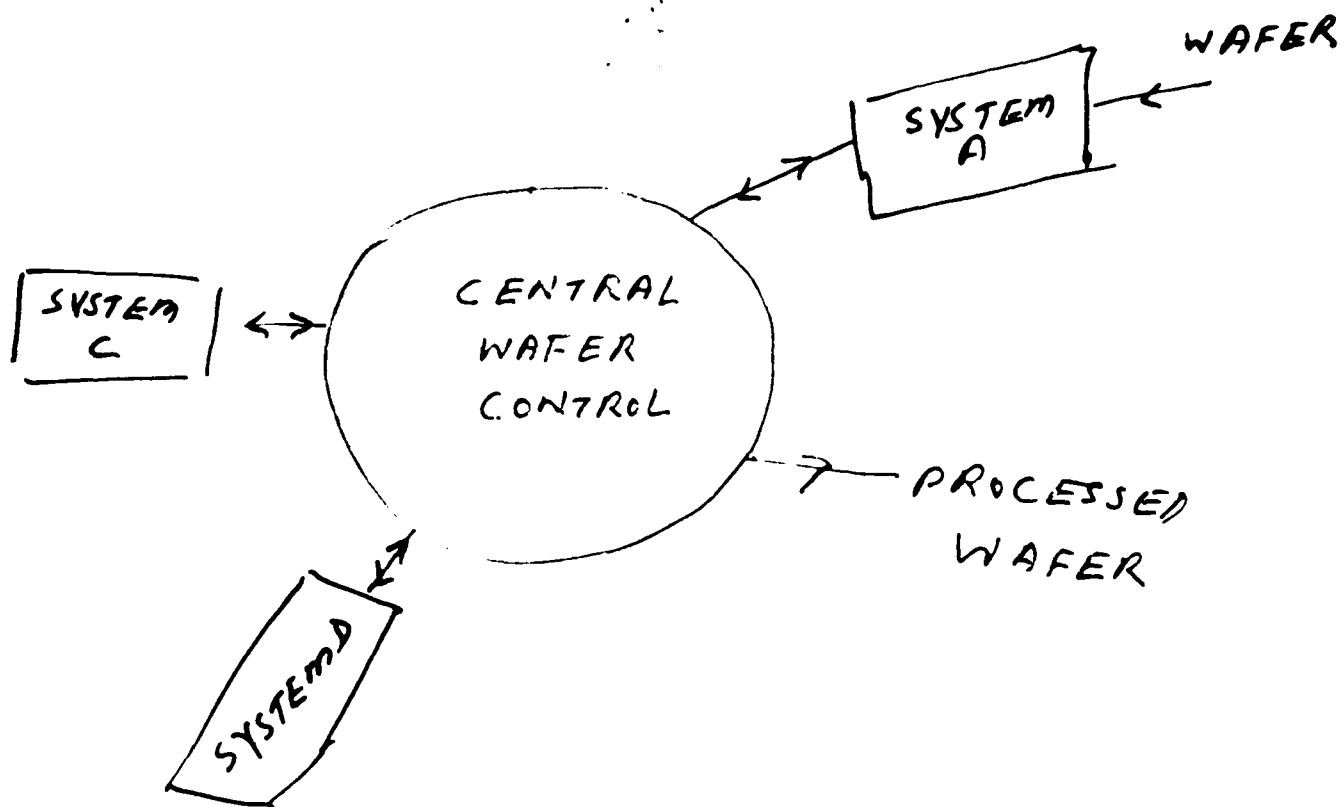
Speed

$$\text{RTT} \approx 3.8ps$$

$$\text{CMOS} \approx 8.0ns$$

PROCESSING

- IN- SITU (CLEAN ROOM NOT A ISSUE)
- ~~SINGLE~~ SINGLE WAFER PROCESSING
- REDUCED TEMPERATURE
  (RAPID ISOTHERMAL PROCESSING
  &
  PLASMA PROCESSING)

- HIGH THROUGHPUT (MOCVD Vs. MBE)

- DIRECT WRITTING
  - ION BEAM
    0.3μm SUP.COND. LINES
  - LASER ? (SPOT SIZE)

- NEW EQUIPMENTS

" EQUIPMENT INDUSTRY "

LITHOGRAPHY - EQUIPMENT
COUPLED WITH PLASMA & RIP

446

MILLIMETER-WAVE InAlAs/InGaAs/InP LATTICE-MATCHED HEMTS

P. C. Chao, K. H G. Duh, P. M. Smith, J. M. Ballingall, P. Ho,
A. Tessmer, M. I. Kao, and A. A. Jabra

Electronics Laboratory
General Electric Company
Syracuse, NY 13221

MILLIMETER-WAVE

InAlAs/InGaAs/InP

LATTICE-MATCHED HEMTs

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J.M. Ballingall, P.Ho, A. Tessmer,
M.I. Kao, and A.A. Jabra

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OUTLINE

- 0.25 and 0.15μm InGaAs/InP LATTICE-MATCHED HEMTs

- DEVICE PERFORMANCE

- InGaAs LATTICE-MATCHED HEMT vs. InGaAs PSEUDOMORPHIC HEMT

- APPLICATIONS AND ISSUES

MATERIAL CHARACTERISTICS OF InGaAs/InP HEMT

GE Aerospace Laboratories

- LARGE CONDUCTANCE BAND DISCONTINUITY

  ΔE_c (AlInAs/InGaAs) $\approx$ 0.5eV FOR HIGH 2DEG CONCENTRATION

- HIGH ELECTRON MOBILITY AND VELOCITY IN InGaAs CHANNEL

  $\mu(300°K) \approx 10,000 \text{ cm}^2/\text{Vs}$

  $v \approx 3 \times 10^7 \text{ cm/s}$

- QUANTUM-WELL CHANNEL CONFINEMENT

InGaAs LATTICE-MATCHED HEMT IS MOST SUITABLE FOR
HIGH-FREQUENCY, HIGH-GAIN AND LOW-NOISE APPLICATIONS.

0.25μm HEMTs - COMPARISON OF NOISE PERFORMANCE

GE Aerospace Laboratories

DEVICE TYPE	18GHz		60GHz	
	F_{min}(dB)	G_a(dB)	F_{min}(dB)	G_a(dB)
AlGaAs/GaAs CONV.	0.7	13.8	1.8	6.4
InGaAs PSEUDOMORPHIC	0.6	14.4	1.8	7.8
InGaAs LATTICE-MATCHED	0.5	15.2	1.2	8.5

InGaAs LATTICE-MATCHED HEMTs PROVIDE SIGNIFICANTLY BETTER NOISE PERFORMANCE AT MMW FREQUENCIES.

MMW PERFORMANCE OF 0.25μm InGaAs/InP HEMT

GE Aerospace Laboratories

GAIN

FREQ.(GHz)	MAG (dB)
63	15.5
95	12.0

- EXTRAPOLATED f_{max} = 380GHz

NOISE

FREQ.(GHz)	F_{min}(dB)	G_a (dB)
18	0.5	15.2
60	1.2	8.5
94	2.1	6.4

POWER

- 150μm GATE-LENGTH HEMT TESTED AT 60GHz.
- OUTPUT POWER   52mW
  POWER DENSITY   0.35W/mm
  EFFICIENCY   23%
  GAIN   3.2dB

18GHz S-PARAMETER - 0.25μm InGaAs LM HEMT vs. PM HEMT

GE Aerospace Laboratories

0.25μm x 50μm

DEVICE TYPE	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
LATTICE-MATCHED	0.8	-99	4.9	96	0.04	38	0.8	-43
PSEUDOMORPHIC	0.8	-97	3.8	97	0.07	33	0.7	-45

WHILE S_{11} AND S_{22} ARE SIMILAR, LATTICE-MATCHED HEMT HAS LARGER S_{21} AND SMALLER S_{12}.

DC/RF PERFORMANCE OF 0.15μm InGaAs/InP HEMT

GE Aerospace Laboratories

NOISE

FREQ.(GHz)	F_{min}(dB)	G_a (dB)
18	0.3	17.1
60	0.9	8.6
94	1.4	6.5

GAIN

FREQ.(GHz)	MAG (dB)
63	16.2
95	12.6

- Extrapolated f_{max} = 405GHz

- Extrinsic f_T = 166GHz (50μm Wide)

- Extrinsic g_m= 1350mS/mm

InGaAs/InP HEMT : TECHNOLOGY ISSUES

- **MATERIAL**

  - DIFFICULT TO GROW HIGH QUALITY AlInAs LAYERS.

- **PROCESSING**

  - InP SUBSTRATE IS VERY FRAGILE, DIFFICULT TO HANDLE WITHOUT BREAKING THE WAFER.

  - CONVENTIONAL HEMT PROCESSING TECHNOLOGY HAS TO BE MODIFIED FOR LATTICE-MATCHED HEMT FABRICATION.

- **RELIABILITY**

  - EXPERIENCED LEAKY GATE - VERY LOW SCHOTTKY FORWARD AND REVERSE BREAKDOWN VOLTAGES, LESS RELIABLE OHMIC CONTACTS

  - THERMALLY UNSTABLE KINK EFFECT IN DRAIN I-V CHARACTERISTICS

InGaAs LATTICE-MATCHED HEMT - APPLICATIONS

GE Aerospace Laboratories

- **LOW-NOISE**

  - STATE-OF-THE-ART NOISE/GAIN PERFORMANCE DEMONSTRATED.

- **HIGH-POWER**

  - HIGH TRANSCONDUCTANCE AND CURRENT DENSITY.

  - TROUBLED BY LEAKY GATE CHARACTERISTICS AND LOW CHANNEL

    BREAKDOWN VOLTAGE

457

SUMMARY

- InGaAS/InP LATTICE-MATCHED HEMTS PROVIDE BETTER MMW NOISE/GAIN PERFORMANCE.

- PRELIMINARY POWER PERFORMANCE IS INFERIOR TO InGaAs PSEUDOMORPHIC HEMTs.

- WORSE RELIABILITY COULD BE EXPECTED IN THE LATTICE-MATCHED HEMT.

MICROWAVE PERFORMANCE AND CIRCUIT APPLICATIONS OF InP/GaInAs HBTS

Leye Aina, Eric A. Martin, Mike Mattingly, Mary Serio,
Erica Hemlpfling, and Lisa Stecker

Allied-Signal Aerospace Company
Aerospace Technology Center
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Columbia, MD 21045

MICROWAVE PERFORMANCE AND CIRCUIT APPLICATIONS OF InP/GaInAs HBTs

BY

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Mary Serio, Erica Hempfling, Lisa Stecker

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Aerospace Technology Center
9140 Old Annapolis Road
Columbia, MD 21045

OUTLINE

- MOTIVATION & JUSTIFICATION

- DC & MICROWAVE PERFORMANCE

- CIRCUIT APPLICATIONS

JUSTIFICATION & APPLICATIONS

- InP/GaInAs HAS THE MOST FAVORABLE PROPERTIES FOR HBTs

  HIGH ΔE_v
  LOW SURFACE STATE DENSITIES

- InP/GaInAs COMPATIBLE WITH OPTIMUM OPTICAL DEVICES

  LASER DIODES & LEDs AT 1.5 - 1.6 μm

- HBTs HAVE UNIQUE APPLICATION NICHES

  HIGH CURRENT DRIVERS FOR LASERS OR LEDs
  THRESHOLD INVARIANT LOGIC DEVICES
  LOW NOISE & HIGH POWER MICROWAVE OSCILLATORS

HBT STRUCTURE AND FABRICATION
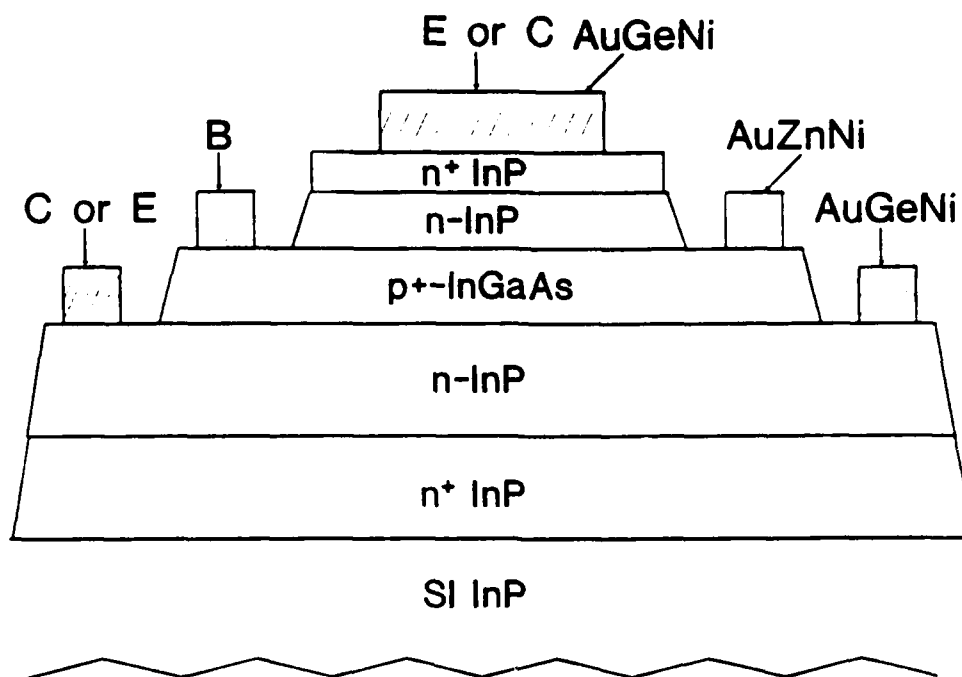
- GROWTH

    OMVPE AT 650°C

    REACTANTS: TMI, TMA, TMG

    DOPANT: Si & Zn

- FABRICATION PROCESS

    ALL MESA ETCHING
    SiO$_2$ PASSIVATION & ISOLATION

    EMITTER & COLLECTOR CONTACTS --- $\rho_c \sim 10^{-6} \Omega$-cm^2
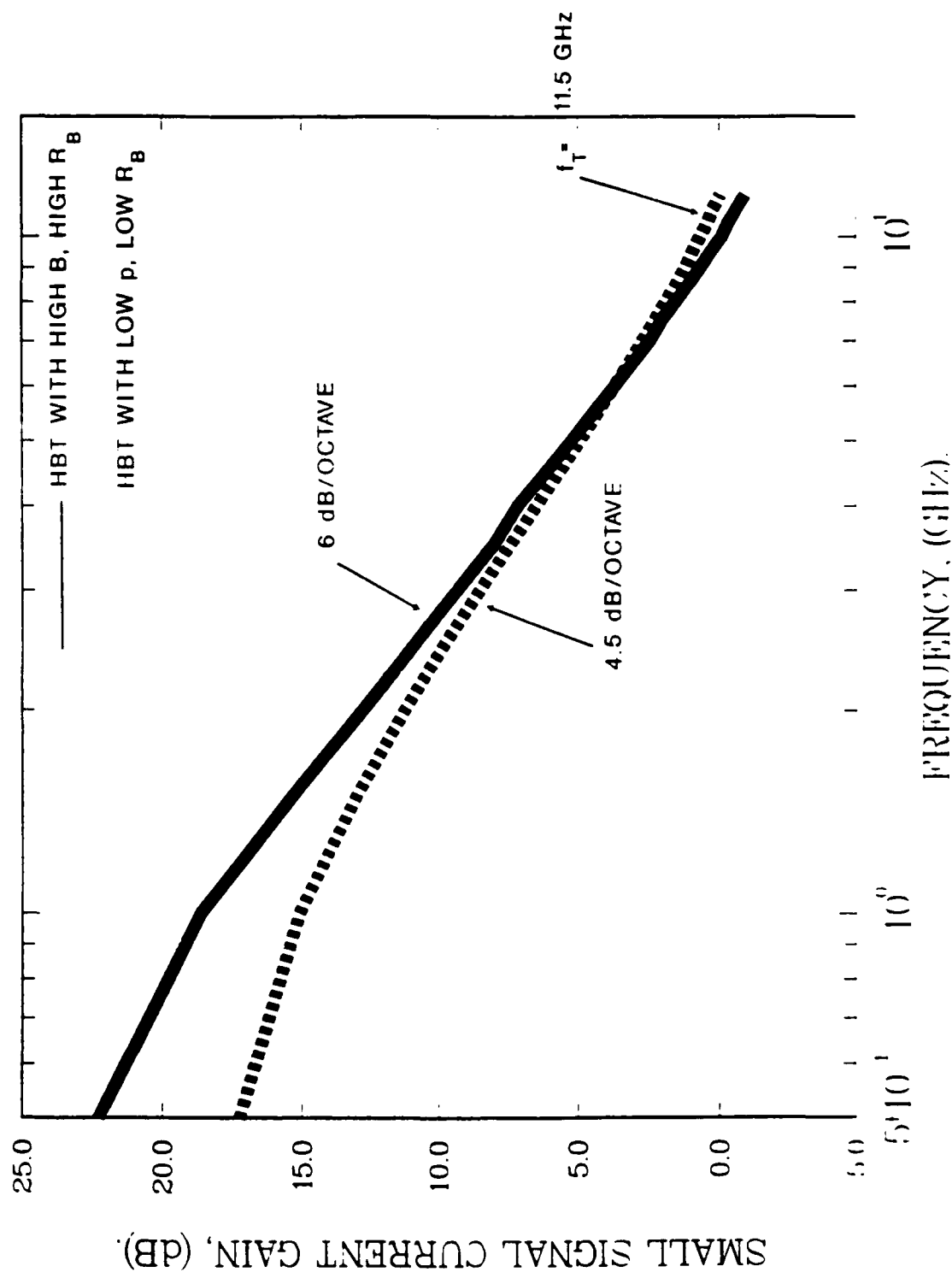   BASE CONTACTS --- $\rho_c \sim 10^{-7} \Omega$-cm^2

TYPICAL HBT LAYOUT
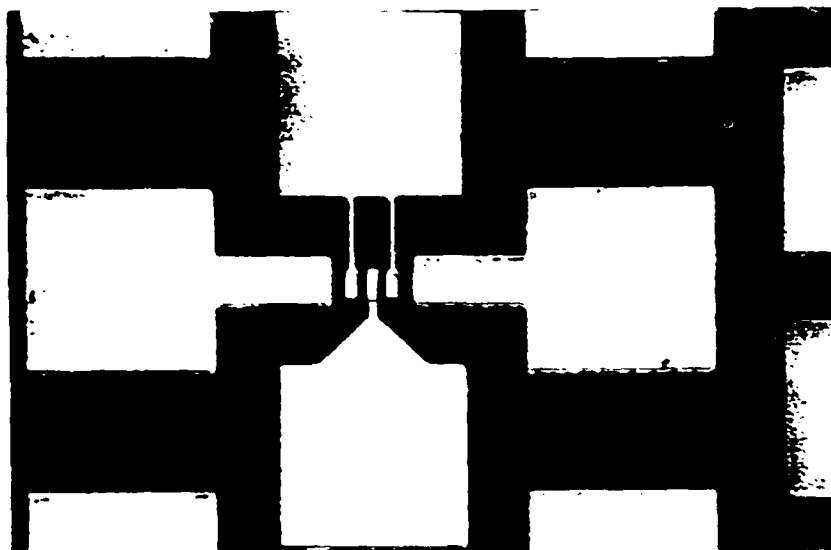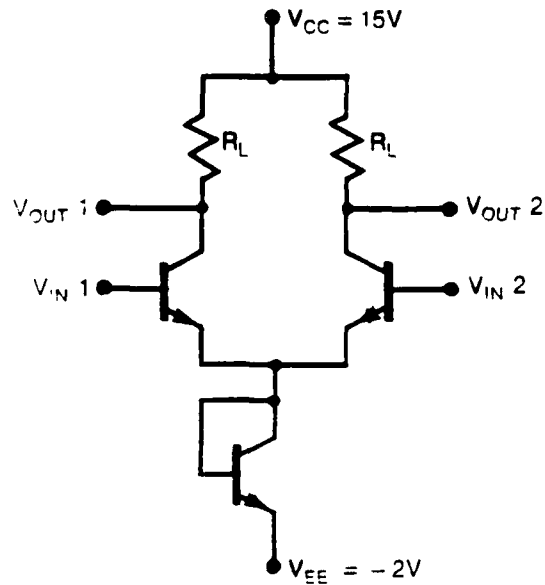

I-V CHARACTERISTICS OF
HBT WITH 5 × 10μm EMITTERS
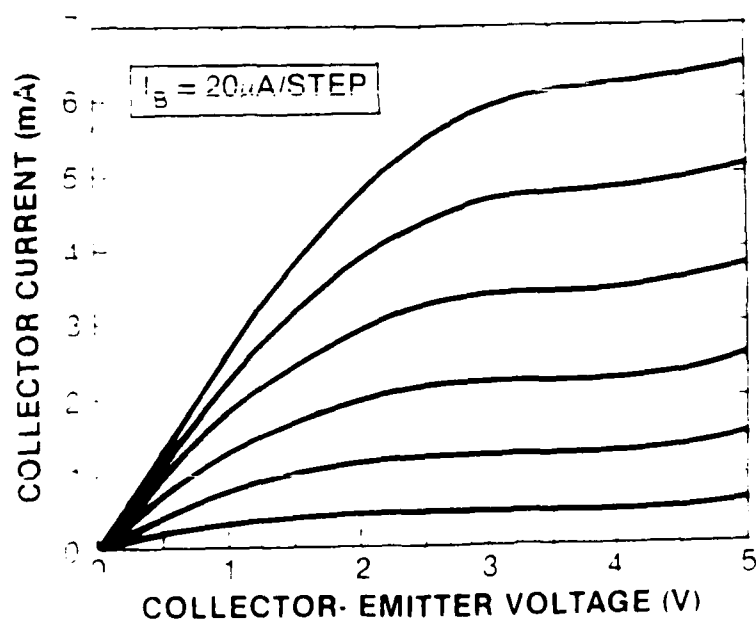
EMITTER DIMENSION DEPENDENCE OF HBTs

$\triangledown$ - AlGaAs/GaAs
$\diamondsuit$ - AlInAs/GaInAs
$\times$ - InP/GaInAs
$|$ - ATC

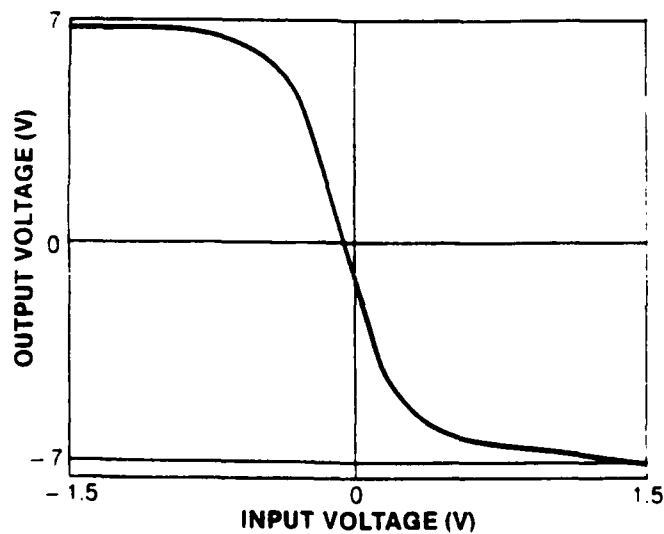SMALL-SIGNAL CURRENT GAIN

PERIMETER/AREA RATIO, (1/MICRON).
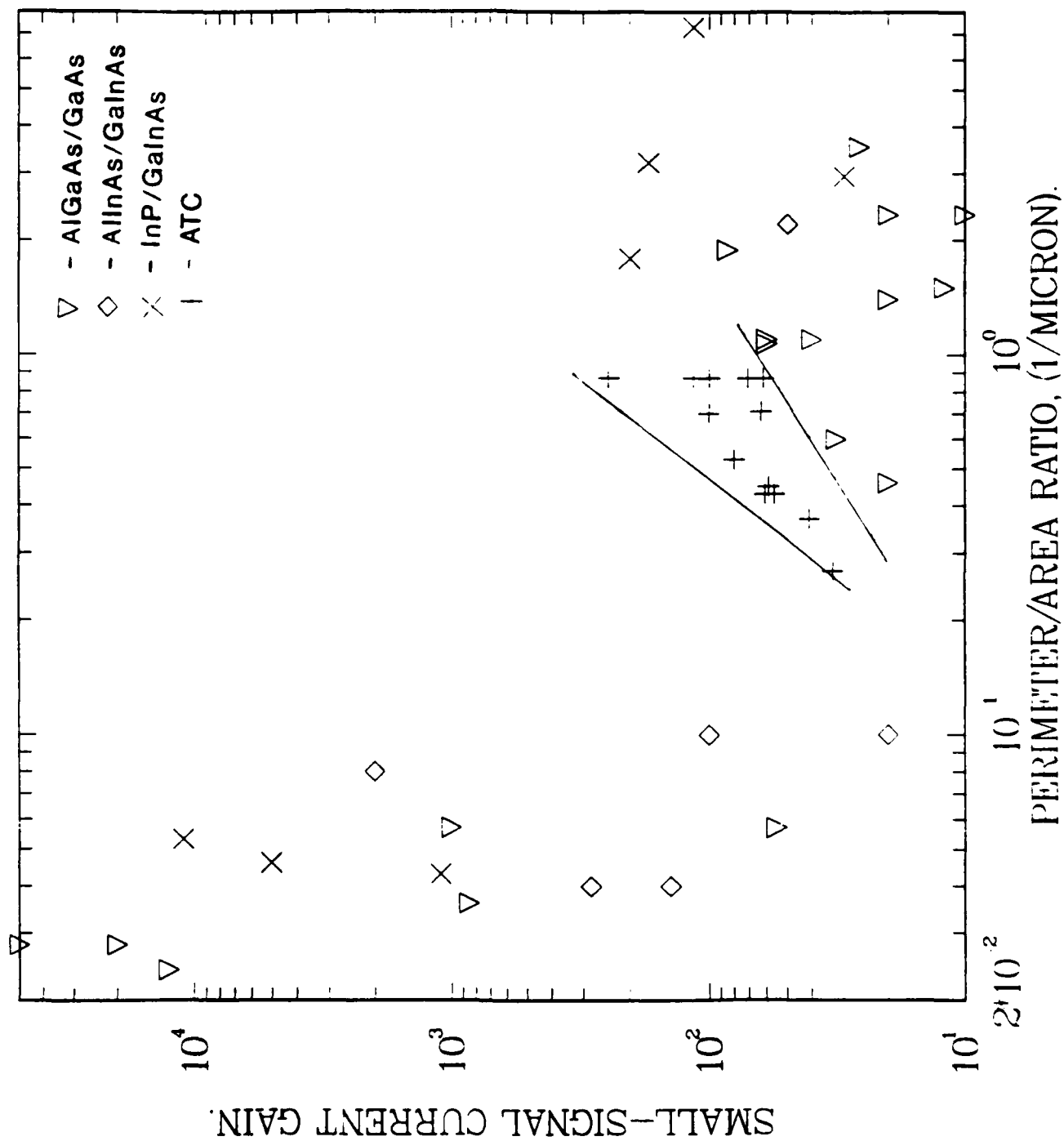
MICROWAVE CURRENT GAINS FOR HBTs WITH 4 X 50 MICRON EMITTERS

CIRCUIT TOPOLOGY OF HBT INVERTER

TRANSFER CHARACTERISTIC OF HBT INVERTER

- VOLTAGE GAIN = 15

- NOISE MARGIN = 6 VOLTS

LAYOUT OF InP/GaInAs HBT INVERTER
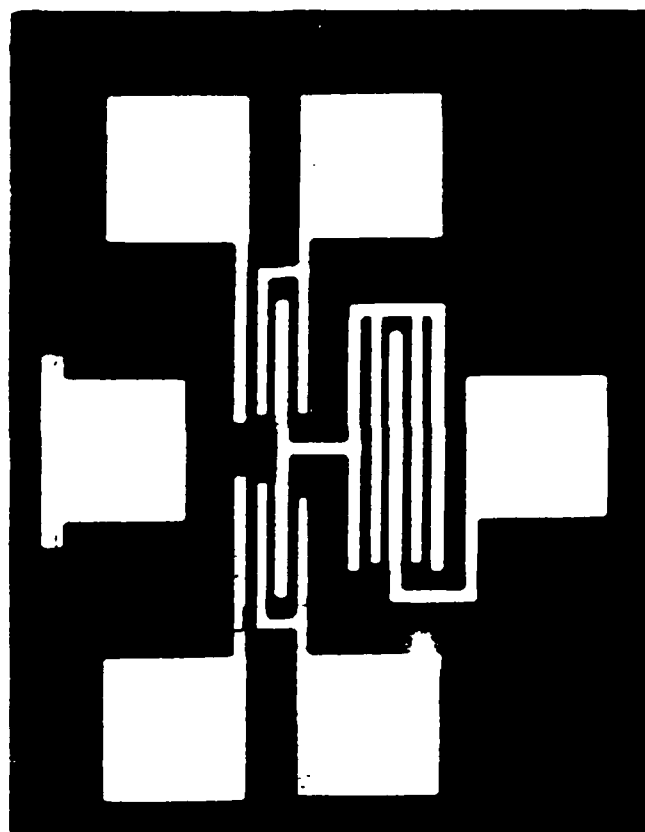
SUMMARY AND FUTURE WORK

- HIGH GAIN InP/GaInAs HBT

  $\beta \sim 240$ FOR SMALL DEVICES

- HIGH f_t FOR A NON-SELF-ALIGNED HBT

  HIGHER FREQUENCY DEVICES NEED A SELF-ALIGNED PROCESS.

- FIRST CIRCUIT APPLICATION OF InP/GaInAs HBT

  ECL INVERTER/DIFF. AMPL. - BASIC BUILDING BLOCK FOR ANALOG & DIGITAL CIRCUITS

MONOLITHIC AND DISCRETE MM-WAVE InP LATERAL TRANSFERRED-ELECTRON OSCILLATORS

S. C. Binari, R. E. Neidert, K. E. Meissner

Naval Research Laboratory
Washington, DC 20375

MONOLITHIC AND DISCRETE MM-WAVE InP LATERAL TRANSFERRED-ELECTRON OSCILLATORS

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NAVAL RESEARCH LABORATORY
WASHINGTON, DC 20375

OUTLINE

- **INTRODUCTION**

- **DISCRETE DEVICE DESIGN AND PERFORMANCE**

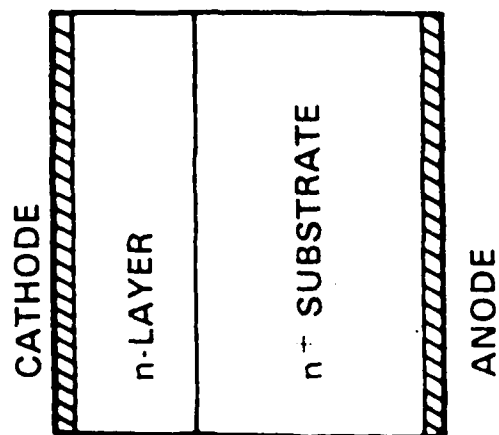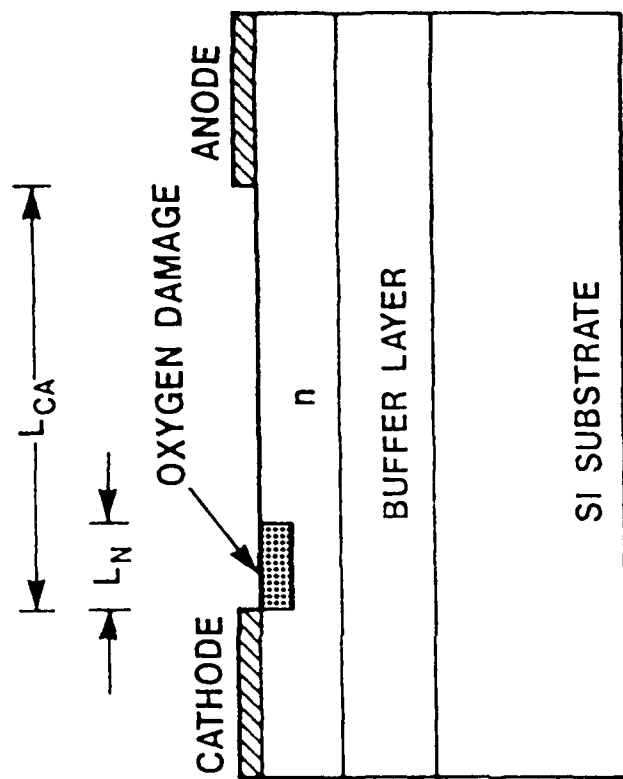- **MONOLITHIC OSCILLATOR DESIGN AND PERFORMANCE**

- **SUMMARY**

InP ADVANTAGES FOR
TRANSFERRED–ELECTRON OSCILLATORS

- HIGHER PEAK–TO–VALLEY VELOCITY RATIO

- LESS TEMPERATURE SENSITIVE PEAK–TO–VALLEY VELOCITY RATIO

- FASTER CENTRAL VALLEY ELECTRON DYNAMICS

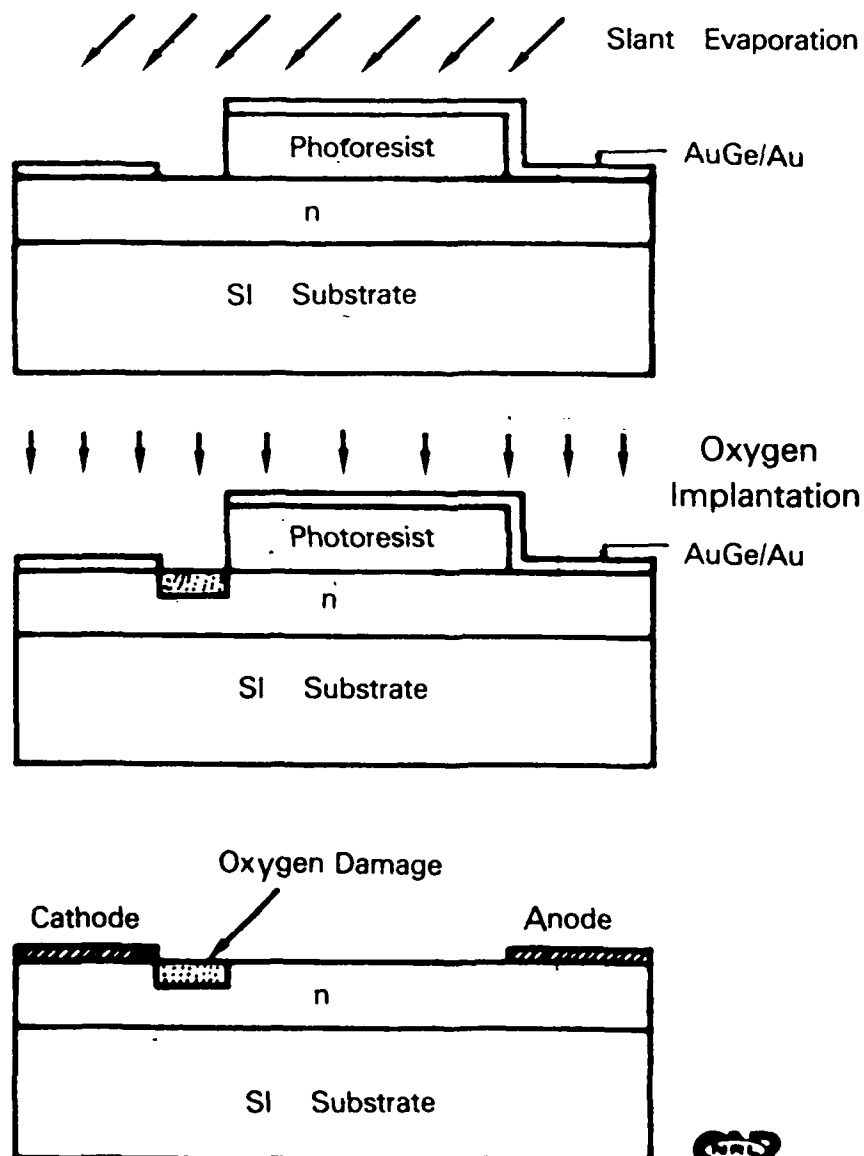- HIGHER THERMAL CONDUCTIVITY
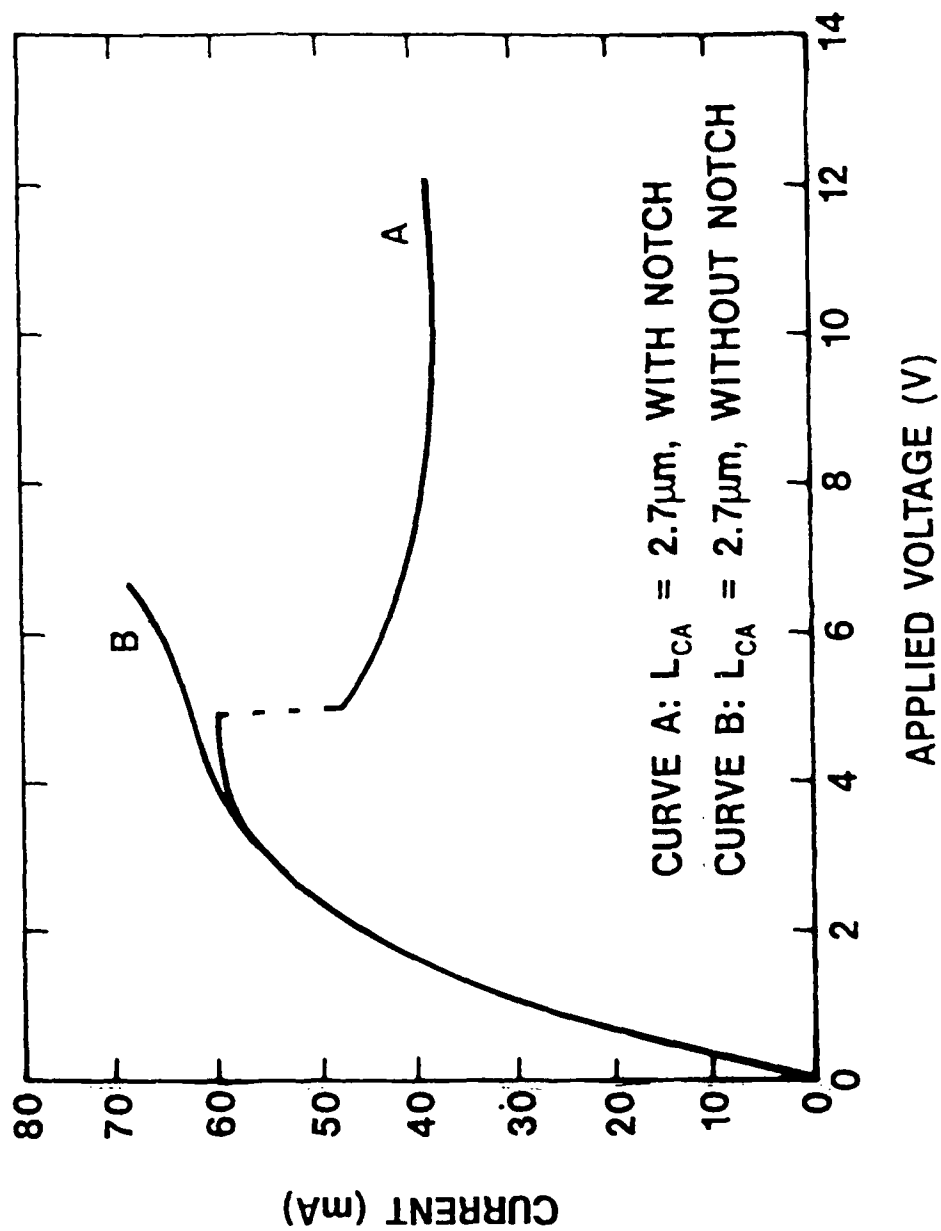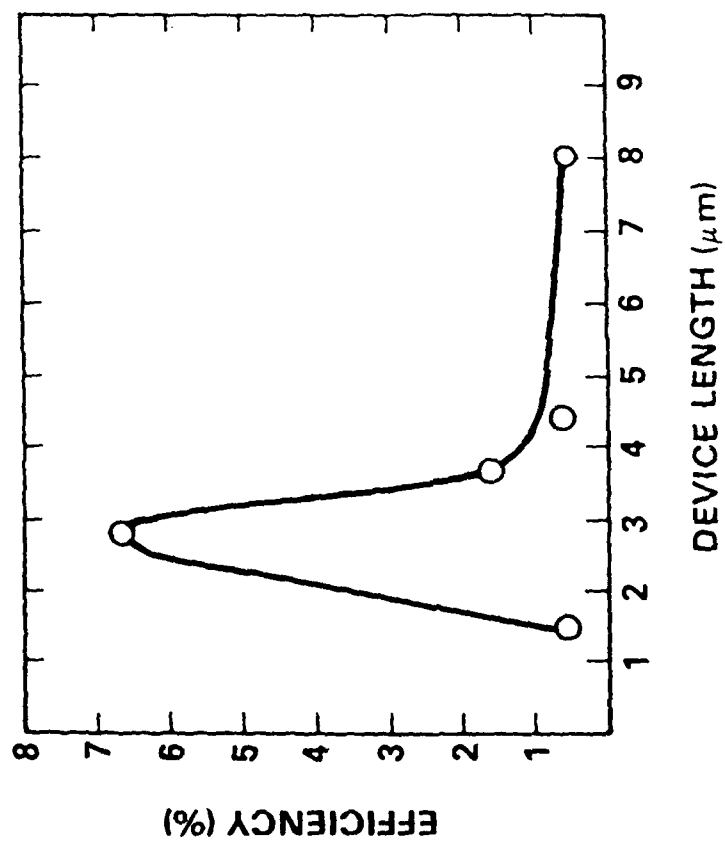
TRANSFERRED-ELECTRON DEVICE STRUCTURES

CATHODE

L_N | L_{CA}

OXYGEN DAMAGE

n

ANODE

BUFFER LAYER

SI SUBSTRATE

LATERAL

CATHODE

n-LAYER

n⁺ SUBSTRATE

ANODE

VERTICAL

SELF-ALIGNED NOTCH
FABRICATION SEQUENCE

Slant Evaporation

Photoresist

AuGe/Au

n

SI Substrate

Oxygen
Implantation

Photoresist

AuGe/Au

n

SI Substrate

Oxygen Damage

Cathode

Anode

n

SI Substrate

DISCRETE DEVICE I–V CHARACTERISTICS

CURVE A: L_{CA} = 2.7μm, WITH NOTCH
CURVE B: L_{CA} = 2.7μm, WITHOUT NOTCH

APPLIED VOLTAGE (V)

CURRENT (mA)

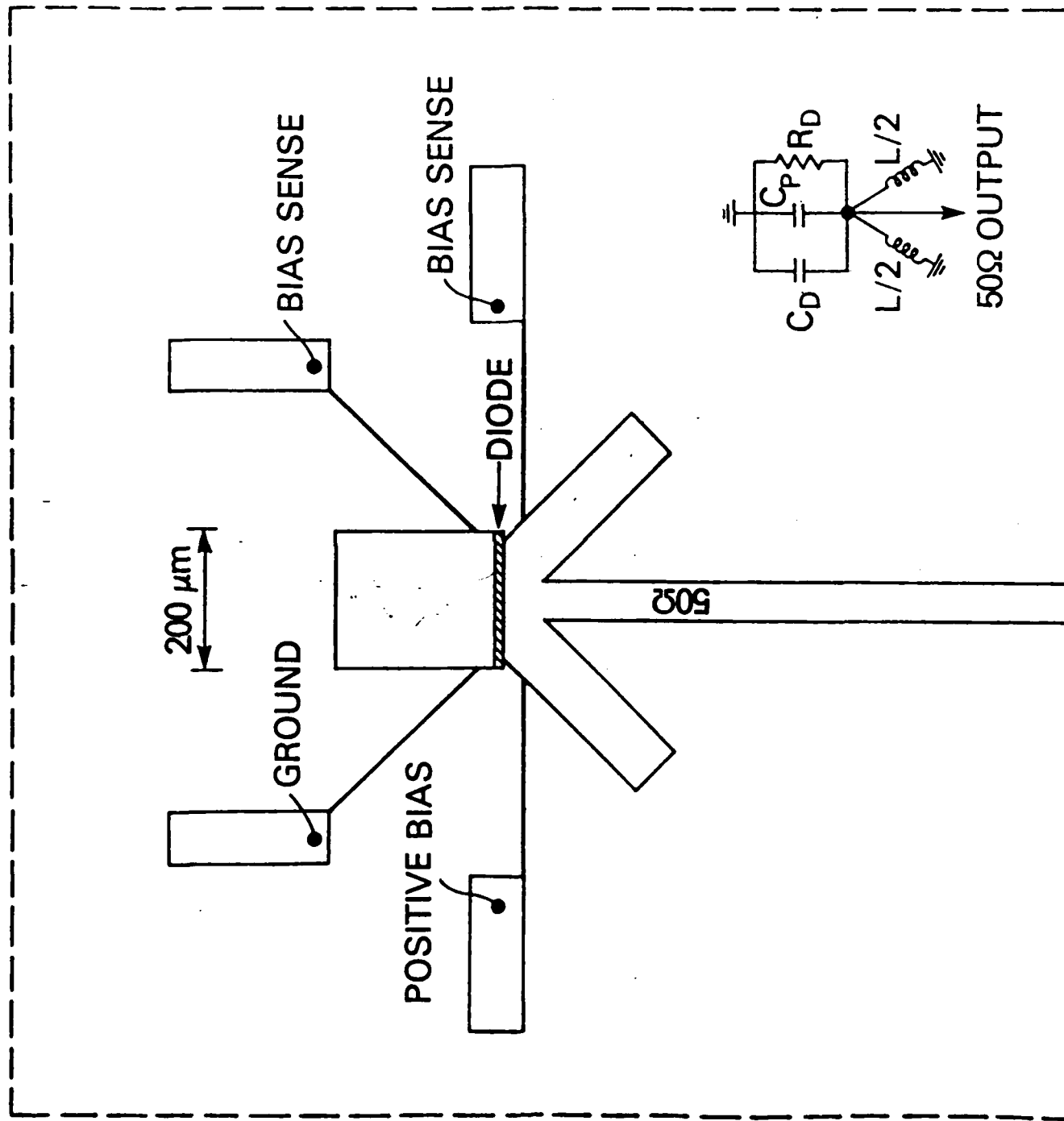# EFFICIENCY VERSUS DEVICE LENGTH AT Ka-BAND

CNR

NON-LTD
DEVICES

479

InP TRANSFERRED-ELECTRON OSCILLATOR DISCRETE DEVICE PERFORMANCE

DEVICE LENGTH, L_{CA} (μm)	FREQUENCY (GHz)	CW POWER (mW)	EFFICIENCY (%)
2.7	29.9	29.1	6.7
1.5	75.2	0.9	0.4
1.5	98.5	0.4	0.2

SUMMARY

- INVESTIGATED A LATERAL DEVICE STRUCTURE
  - KEY DESIGN FEATURE IS HIGH RESISTIVITY NOTCH
  - EASILY INTEGRATED INTO MONOLITHIC CIRCUIT

- DISCRETE DEVICES IN TUNABLE WAVEGUIDE CAVITIES
  - HIGHEST REPORTED EFFICIENCY OF 6.7% WITH 29.1 mW AT 29.9 GHz
  - HIGHEST FREQUENCY OSCILLATIONS
    0.9 mW AT 75.2 GHz
    0.4 mW AT 98.5 GHz

- DEMONSTRATED FIRST MONOLITHIC OSCILLATOR INCORPORATING A LATERAL TED
  0.1 mW POWER OUTPUT AT 79.9 GHz

REPORT DOCUMENTATION PAGE

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13. ABSTRACT *(Maximum 200 words)*

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14. SUBJECT TERMS

indium phosphide (InP) microwave
MISFETs milliwave
optoelectronics

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